TLV320AIC34EVM-K

This user's guide describes the characteristics, operation, and use of the TLV320AIC34EVM-K. This evaluation module (EVM) allows the user to evaluate the TLV320AIC34 audio codec. The TLV320AIC34 is a complete 4-channel audio codec with several inputs and outputs, extensive audio routing, mixing and effects capabilities. A complete circuit description, schematic diagram and bill of materials are also included. Note that the TLV320AIC34 only uses the I^2C bus for register control. Any references to the SPI control bus in this document is due to the presence of this interface on the USB-MODEVM motherboard.

The following related documents are available through the Texas Instruments web site at www.ti.com.

EVM-Compatible Device Data Sheets

Device	Literature Number
TLV320AIC34	SLAS538
TAS1020B	SLES025
REG1117-3.3	SBVS001
TPS767D318	SLVS209
SN74LVC125A	SCAS290
SN74LVC1G125	SCES223
SN74LVC1G07	SCES296

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1 EVM Overview

1.1 Features

- Full-featured evaluation board for the TLV320AIC34 4-channel audio codec.
- Modular design for use with a variety of digital signal processor (DSP) and microcontroller interface boards.
- USB connection to PC provides power, control, and streaming audio data for easy evaluation.
- On-board microphone for ADC evaluation
- Connection points for external control and digital audio signals for quick connection to other circuits/input devices.

The TLV320AIC34EVM-K is a complete evaluation kit, which includes a universal serial bus (USB)-based motherboard and evaluation software for use with a personal computer running the Microsoft Windows™ operating system (Win2000 or XP).

1.2 Introduction

The TLV320AIC34EVM is in Texas Instruments' modular EVM form factor, which allows direct evaluation of the device performance and operating characteristics, and eases software development and system prototyping. This EVM is compatible with the 5-6K Interface Evaluation Module (SLAU104) and the HPA-MCUINTERFACE (SLAU106) from Texas Instruments and additional third-party boards which supports the TI Modular EVM format.

The TLV320AIC34EVM-K is a complete evaluation/demonstration kit, which includes a USB-based motherboard called the USB-MODEVM Interface board and evaluation software for use with a personal computer running the Microsoft Windows operating systems.

The USB connection from the PC provides power, control, and streaming audio data to the EVM for reduced setup and configuration. The EVM also allows external control signals, audio data, and power for advanced operation, which allows prototyping and connection to the rest of the evaluation/development system.

2 EVM Description and Basics

This section provides information on the analog input and output, digital control, power and general connection of the TLV320AIC34EVM.

2.1 TLV320AIC34EVM-K Block Diagram

The TLV320AIC34EVM-K consists of two separate circuit boards, the USB-MODEVM and the TLV320AIC34EVM. The USB-MODEVM is built around a TAS1020B streaming audio USB controller with an 8051-based core.

The simple diagram below (Figure 1) shows the how the TLV320AIC34EVM is connected to the USB-MODEVM. The USB-MODEVM Interface board is intended to be used in USB mode, where control of the installed EVM is accomplished using the onboard USB controller device. Provision is made, however, for driving all the data buses (I^2C, I^2S, etc.) externally. The source of these signals is controlled by SW2 on the USB-MODEVM. Refer to Table 1 for details on the switch settings.

2.1.1 USB-MODEVM Interface Board

The simple diagram shown in Figure 1 shows only the basic features of the USB-MODEVM Interface board.

When connecting the TLV320AIC34EVM to the USB-MODEVM care must be used to avoid bending the connecting pins. The two boards can only be connected in one way. It is suggested to first align with the 10-pin connectors (J15B on the TLV320AIC34EVM and J18A on the USB-MODEVM) and then gently push all the connectors together until the boards are seated.

In the factory configuration, the board is ready to use with the TLV320AIC34EVM. To view all the functions and configuration options available on the USB-MODEVM board, see the USB-MODEVM Interface Board schematic in Appendix.

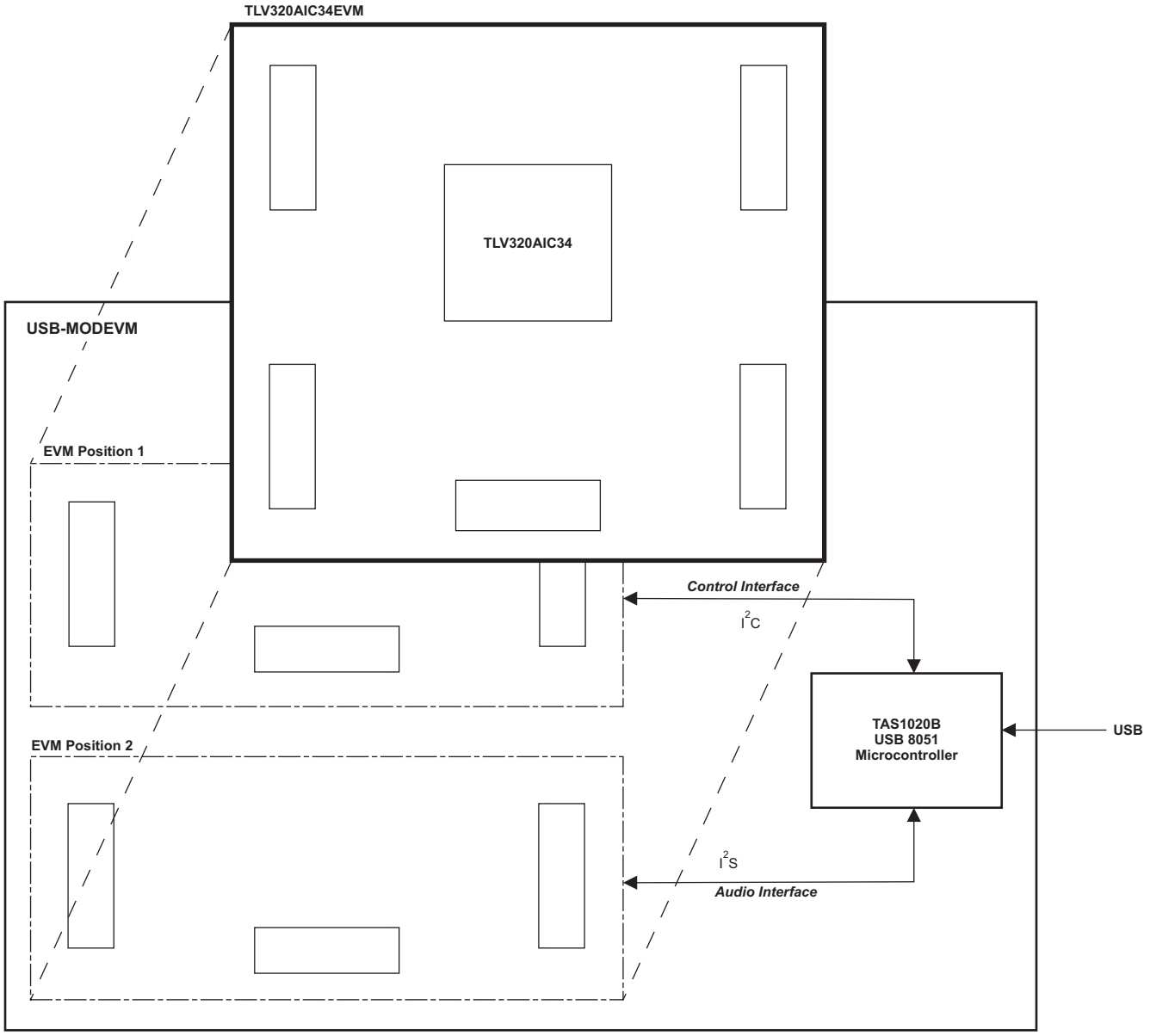


Figure 1. TLV320AIC34EVM-K Block Diagram

2.2 Default Configuration and Connections

2.2.1 USB-MODEVM

Table 1 provides a list of the SW2 settings on the USB-MODEVM. For use with the TLV320AIC34EVM, SW-2 positions 1 through 7 should be set to ON (LO), while SW-2.8 should be set to OFF (HI).

Table 1. USB-MODEVM SW2 Settings

SW-2 Switch Number	Label	Switch Description
1	A0	USB-MODEVM EEPROM I^2C Address A0 ON: A0 = 0 OFF: A0 = 1
2	A1	USB-MODEVM EEPROM I^2C Address A1 ON: A1 = 0 OFF: A1 = 1
3	A2	USB-MODEVM EEPROM I^2C Address A2 ON: A2 = 0 OFF: A2 = 1
4	USB I^2S	I^2S Bus Source Selection ON: I^2S Bus connects to TAS1020 OFF: I^2S Bus connects to USB-MODEVM J14
5	USB MCK	I^2S Bus MCLK Source Selection ON: MCLK connects to TAS1020 OFF: MCLK connects to USB-MODEVM J14
6	USB SPI	SPI Bus Source Selection ON: SPI Bus connects to TAS1020 OFF: SPI Bus connects to USB-MODEVM J15
7	USB RST	RST Source Selection ON: EVM Reset Signal comes from TAS1020 OFF: EVM Reset Signal comes from USB-MODEVM J15
8	EXT MCK	External MCLK Selection ON: MCLK Signal is provided from USB-MODEVM J10 OFF: MCLK Signal comes from either selection of SW2-5

2.2.2 TLV320AIC34EVM Jumper Locations

Table 2 and Table 3 provide a list of jumpers found on the EVM and their factory default conditions.

Table 2. List of Standalone Jumpers

Jumper	Default Position	Jumper Description
JMP1	2-3	When connecting 2-3, mic bias comes from the MICBIAS pin on the device; when connecting 1-2, mic bias is supplied from the power supply through a resistor, which the user must install.
JMP2	Installed	Connects on-board Mic to Left Microphone Input.
JMP3	Installed	Connects on-board Mic to Right Microphone Input.
JMP4	Installed	Provides a means of measuring IOVDD current.
JMP5	soldered	DRVDD power.
JMP6	soldered	DVDD power.
JMP7	soldered	DRVDD power.
JMP8	soldered	AVDD_DAC power.
JMP9	Installed	Connects Analog and Digital Grounds.
JMP10	Open	When installed, shorts across the output capacitor on HPLOUT_A; remove this jumper if using AC-coupled output drive.
JMP11	Open	When installed, shorts across the output capacitor on HPLCOM_A; remove this jumper if using AC-coupled output drive.
JMP12	Open	When installed, shorts across the output capacitor on HPROUT_A; remove this jumper if using AC-coupled output drive.
JMP13	Open	When installed, shorts across the output capacitor on HPLOUT_B; remove this jumper if using AC-coupled output drive.
JMP14	Open	When installed, shorts across the output capacitor on HPLCOM_B; remove this jumper if using AC-coupled output drive.
JMP15	Open	When installed, shorts across the output capacitor on HPROUT_B; remove this jumper if using AC-coupled output drive.

Table 2. List of Standalone Jumpers (continued)

Jumper	Default Position	Jumper Description
JMP16	Installed	When installed, shorts HPLCOM_A and HPRCOM_A. Use only if these signals are set to constant VCM and external feedback. Also, switch SW1 must be in the "Capless" position when installed.
JMP17	Open	When installed, shorts across the output capacitor on HPRCOM_A; remove this jumper if using AC-coupled output drive.
JMP18	Open	Selects on-board EEPROM as Firmware Source. Note that for this EVM the Firmware Source EEPROM is on the USB-MODEVM.
JMP19	Installed	When installed, allows the USB-MODEVM to hardware reset the device under user control
JMP20	Installed	When installed, shorts HPLCOM_B and HPRCOM_B. Use only if these signals are set to constant VCM and external feedback.
JMP21	Open	When installed, shorts across the output capacitor on HPRCOM_B; remove this jumper if using AC-coupled output drive.

Table 3. List of Jumpers Connected to J17A (Digital Interface Signals)

Signals	J17A Default Position	Jumper Description
BCLK_A and BCLK_B	pin 3 - pin 5	Connects Block A BCLK_A and Block B BLCK_B together for ease of evaluation. **When Block A and Block B use different digital clocks/data this jumper MUST be removed.**
WCLK_A and WCLK_B	pin 7 - pin 9	Connects Block A WCLK_A and Block B WLCK_B together for ease of evaluation. **When Block A and Block B use different digital clocks/data this jumper MUST be removed.**
DIN_A and DIN_B	pin 10 - pin 11	Connects Block A DIN_A and Block B DIN_B together for ease of evaluation. **When Block A and Block B use different digital clocks/data this jumper MUST be removed.**
DOUT_A and DOUT_B	open	Connects Block A DOUT_A and Block B DOUT_B together for ease of evaluation. **When Block A and Block B use different digital clocks/data this jumper MUST be removed. Also if both Block A and Block B are used together this jumper must be removed due to potential conflict on the DOUT signals.**
MCLK_A and MCLK_B	pin 17 - pin 19	Connects Block A MCLK_A and Block B MCLK_B together for ease of evaluation. **When Block A and Block B use different digital clocks/data this jumper MUST be removed.**.

2.3 Block A Analog Signal Connections

2.3.1 Block A Analog Inputs

The Block A analog inputs to the EVM can be connected through the analog headers J1, J2, J3, J4, J5, and J6 around the edge of the board. The connection details of each header/connector can be found in Table A-2.

2.3.2 Block A Analog Output

The Block A analog outputs to the EVM can be connected through J7, J8, J9, J11,and J12 at the edges of the board. The connection details can be found in Table A-2.

2.4 Block A Digital Signal Connections

2.4.1 Block A Digital Inputs and Outputs

The digital inputs and outputs of the EVM can be monitored through J16 and J17. If external signals need to be connected to the EVM, digital inputs should be connected via J14 and J15 on the USB-MODEVM and the SW2 switch should be changed accordingly (see Section 2.2.1). The connector details are available in Section A.2.

2.4.2 Block A Digital Controls

The digital control signals can be applied directly to J16 and J17 (top or bottom side). The modular TLV320AIC34EVM can also be connected directly to a DSP interface board, such as the 5-6KINTERFACE or HPA-MCUINTERFACE, or to the USB-MODEVM Interface board (included in this EVM kit).

2.5 Block B Analog Signal Connections

2.5.1 Block B Analog Inputs

The Block B analog inputs to the EVM can be applied directly to J13 (top or bottom side). The connection details of each header/connector can be found in Table A-1.

2.5.2 Block B Analog Output

The Block B analog outputs to the EVM can be connected through J13 and J14 (top or bottom). The connection details can be found in Table A-1.

2.6 Block B Digital Signal Connections

2.6.1 Block B Digital Inputs and Outputs

The digital inputs and outputs of the EVM can be monitored through J16 and J17. If external signals need to be connected to the EVM, digital inputs should be connected via J14 and J15 on the USB-MODEVM and the SW2 switch should be changed accordingly (see Section 2.2.1). The connector details are available in Section A.2.

2.6.2 Block B Digital Controls

The digital control signals can be applied directly to J16 and J17 (top or bottom side). The modular TLV320AIC34EVM can also be connected directly to a DSP interface board, such as the 5-6KINTERFACE or HPA-MCUINTERFACE, or to the USB-MODEVM Interface board (included in this EVM kit).

2.7 Power Connections

The TLV320AIC34 can be powered independently when being used in stand-alone operation or by the USB-MODEVM when it is plugged onto the motherboard.

2.7.1 Stand-Alone Operation

When used as a stand-alone , power is applied to J15 directly, making sure to reference the supplies to the appropriate grounds on that connector.

CAUTION

Before applying power to the EVM you **must** verify that all power supplies are within the **safe operating limits** as indicated in the TLV320AIC34 data sheet.

J15 provides connection to the common power bus for the TLV320AIC34EVM. Power is supplied on the pins listed in Table A-4.

The TLV320AIC34EVM-K motherboard (the USB-MODEVM Interface board) supplies power to J15 of the TLV320AIC34EVM. Power for the motherboard is supplied either through its USB connection or via terminal blocks on that board.

2.7.2 USB-MODEVM Operation

The USB-MODEVM Interface board can be powered from several different sources:

- USB
- 6Vdc-10Vdc AC/DC external wall supply (not included)
- Lab power supply

When powered from the USB connection, JMP6 should have a shunt from pins 1–2 (this is the default factory configuration). When powered from 6V-10Vdc, either through the J8 terminal block or J9 barrel jack, JMP6 should have a shunt installed on pins 2–3. If power is applied in any of these ways, onboard regulators generate the required supply voltages and no further power supplies are necessary.

If lab supplies are used to provide the individual voltages required by the USB-MODEVM Interface, JMP6 should have no shunt installed. Voltages are then applied to J2 (+5VA), J3 (+5VD), J4 (+1.8VD), and J5 (+3.3VD). The +1.8VD and +3.3VD can also be generated on the board by the onboard regulators from the +5VD supply; to enable this configuration, the switches on SW1 need to be set to enable the regulators by placing them in the ON position (lower position, looking at the board with text reading right-side up). If +1.8VD and +3.3VD are supplied externally, disable the onboard regulators by placing SW1 switches in the OFF position.

Each power supply voltage has an LED (D1-D7) that lights when the power supplies are active.

3 TLV320AIC34EVM-K Setup and Installation

The following section provides information on using the TLV320AIC34EVM-K, including set up, program installation, and program usage.

Note: If using the EVM in stand-alone mode, the software should be installed per below, but the hardware configuration may be different.

3.1 Software Installation

1. Locate installation file on the CD-ROM include with the EVM or download the latest version of the software located on the AIC34 Product Page.
2. Unzip the installation file by clicking on the self-extracting zip file.
3. Install the EVM software by double-clicking the **Setup** executable and follow the directions. The user may be prompted to restart their computer.

This should install all the TLV320AIC34 software and required drivers onto the PC.

3.2 EVM Connections

1. Ensure that the TLV320AIC34EVM is installed on the USB-MODEVM Interface board, aligning J13, J14, J15, J16, J17 with the corresponding connectors on the USB-MODEVM.
2. Verify that the jumpers and switches are in their default conditions.
3. Attach a USB cable from the PC to the USB-MODEVM Interface board. The default configuration will provide power, control signals, and streaming audio via the USB interface from the PC. On the USB-MODEVM, LEDs D3-6 should light to indicate the power is being supplied from the USB.
4. For the first connection, the PC should recognize new hardware and begin an initialization process. The user may be prompted to identify the location of the drivers or allow the PC to automatically search for them. Allow the automatic detection option.
5. Once the PC confirms that the hardware is operational, D2 on the USB-MODEVM should light to indicate that the firmware has been loaded and the EVM is ready for use. If the LED is not lighted, verify that the drivers were installed and trying to unplug and restart at Step 3.

After the TLV320AIC34EVM-K software installation (described in Section 3.2) is complete, evaluation and development using the target TLV320AIC34 can begin.

The TLV320AIC34EVM software can now be launched. The user should see an initial screen that looks similar to Figure 2.

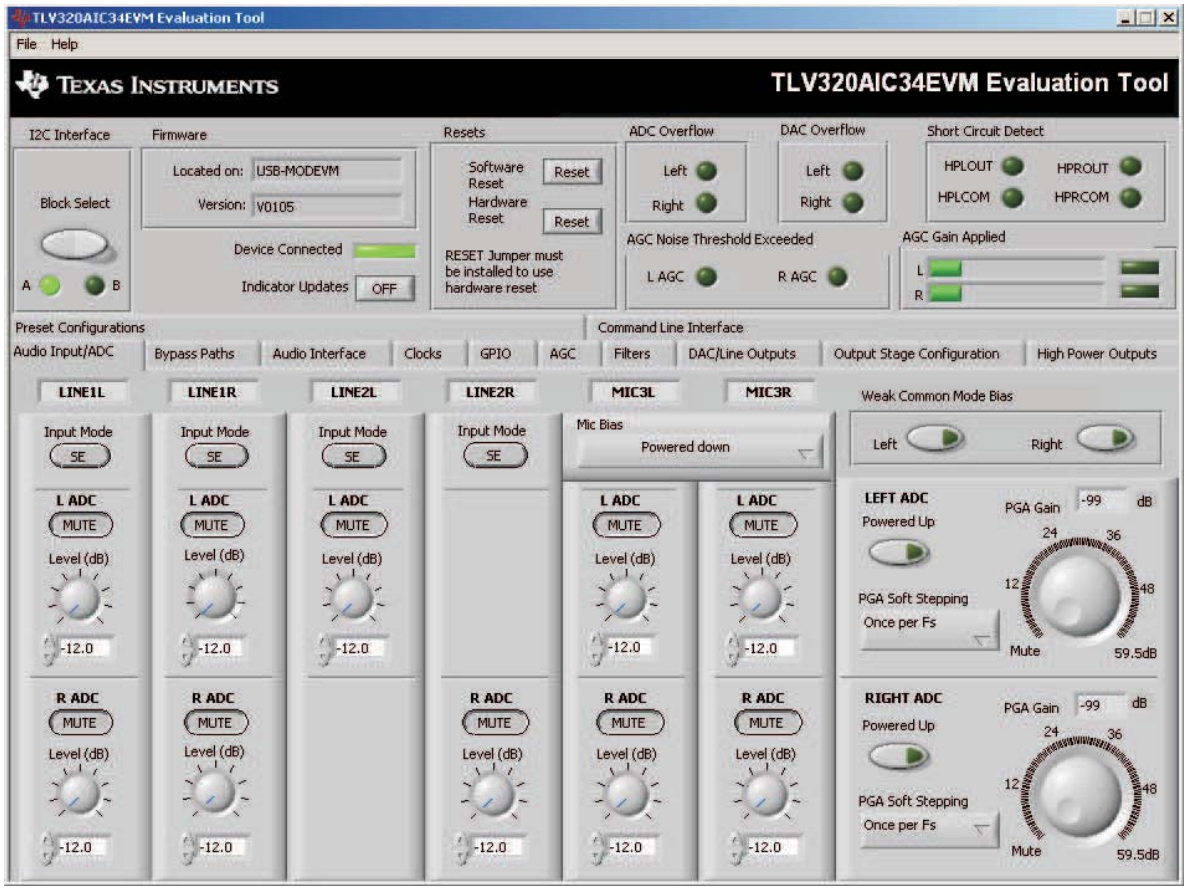


Figure 2. Default Software Screen

4 TLV320AIC34EVM Software

The following section discusses the details and operation of the EVM software.

Note: For configuration of the codec, the TLV320AIC34 block diagram located in the TLV320AIC34 data sheet is a good reference to help determine the signal routing.

4.1 I^2C Address Selection

When the software is run, a window appears which allows for selecting the I^2C address of the TLV320AIC34. This window (see Figure 3) has two controls for setting the state of **ADDR_A** and **ADDR_B**. To allow proper communication with the EVM, these should match the settings of SW2 located on the EVM (Table 2). When **ADDR_A** and **ADDR_B** are adjusted, the correct device address for Block A and Block B will be shown. Note that the actual I^2C address shown and the address for the software may be different. This is done for programming reasons and the correct address should be used for system development.

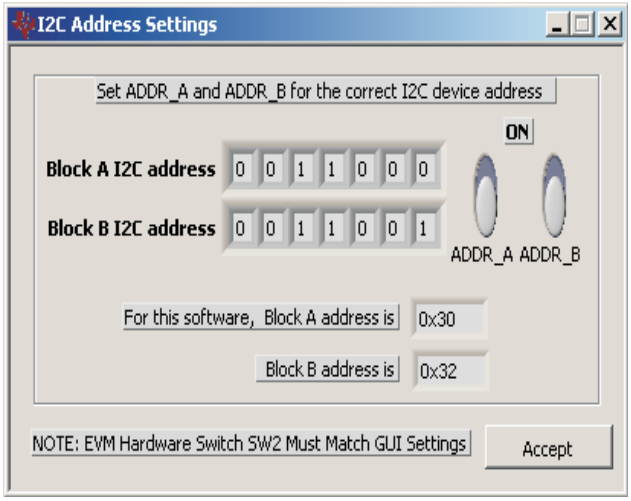


Figure 3. I^2C Address Selection Window

Note: For operation of the EVM in the default state, no changes are required on this panel. The default setting for the GUI software and the default setting for the EVM hardware are configured so that Block A address is 0x30 and Block B address is 0x32 as shown. This corresponds to SW2 on the TLV320AIC34EVM being in position LO-LO.

4.2 Front Page Indicators and Functions

Figure 2 illustrates the main screen of the EVM software. The indicators and buttons located above the tabbed section of the front page are visible regardless of which tab is currently being selected.

At the top left of the screen is an **Block Select** control. This control allows the user to select either Block A or Block B as the target for the GUI controls. When the Block A indicator is green the register writes use the I2C address for Block A. Likewise, When the Block B indicator is green the register writes use the I2C address for Block B.

To the right of the Block Select control is a group box called Firmware . This box indicates where the firmware being used is operating from—in this release, the firmware is on the USB-MODEVM, so the user should see *USB-MODEVM* in the box labeled **Located On:**. The version of the firmware appears in the **Version** box below this.

To the right, the next group box contains controls for resetting the TLV320AIC34EVM. A software reset can be done by writing to a register in the TLV320AIC34EVM, and this is accomplished by pushing the button labeled **Software Reset**. The TLV320AIC34EVM also may be reset by toggling a pin on the TLV320AIC34EVM, which is done by pushing the **Hardware Reset** button. JMP19 on the EVM is installed to allow the reset to reach the TLV320AIC34.

CAUTION

The GUI software does NOT keep track of register settings when toggling between Block A and Block B. When using both Block A and Block B register updates it is recommended to either use I^2C scripts for both blocks or use GUI controls for one block and I^2C scripts for the other block. **Toggling between Block A and Block B is not recommended**.

Below the **Firmware** box, the **Device Connected** LED should be green when the EVM is connected. If the indicator is red, the EVM is not properly connected to the PC. Disconnect the EVM and verify that the drivers were correctly installed, then reconnect and try restarting the software.

One the upper right portion of the screen, several indicators are located which provide the status of various portions of the TLV320AIC34. These indicators are activated by pressing the **Indicator Updates** button below the **Device Connected** LED. These indicators, as well as the other indicators on this panel, are updated only when the software's front panel is inactive, once every 20ms.

The **ADC Overflow** and **DAC Overflow** indicators light when the overflow flags are set in the TLV320AIC34. Below these indicators are the **AGC Noise Threshold Exceeded** indicators that show when the AGC noise threshold is exceeded. To the far right of the screen, the **Short Circuit Detect** indicators show when a short-circuit condition is detected, if this feature has been enabled. Below the short-circuit indicators, the **AGC Gain Applied** indicators use a bar graph to show the amount of gain which has been applied by the AGC, and indicators that light when the AGC is saturated.

4.3 Default Configuration (Presets) Tab

The Default Configuration Tab Figure 4 provides several different preset configurations of the codec. The **Preset Configurations** buttons allow the user to choose from the provided defaults. When the selection is made, the **Preset Configuration Description** are shows a summary of the codec setup associated with the choice made. If the choice is acceptable, the **Load** button can be pressed and the preset configuration will be loaded into the codec. The user can change to the **Command Line Interface** Tab (see Figure 27) to view the actual settings that were programmed into the codec.

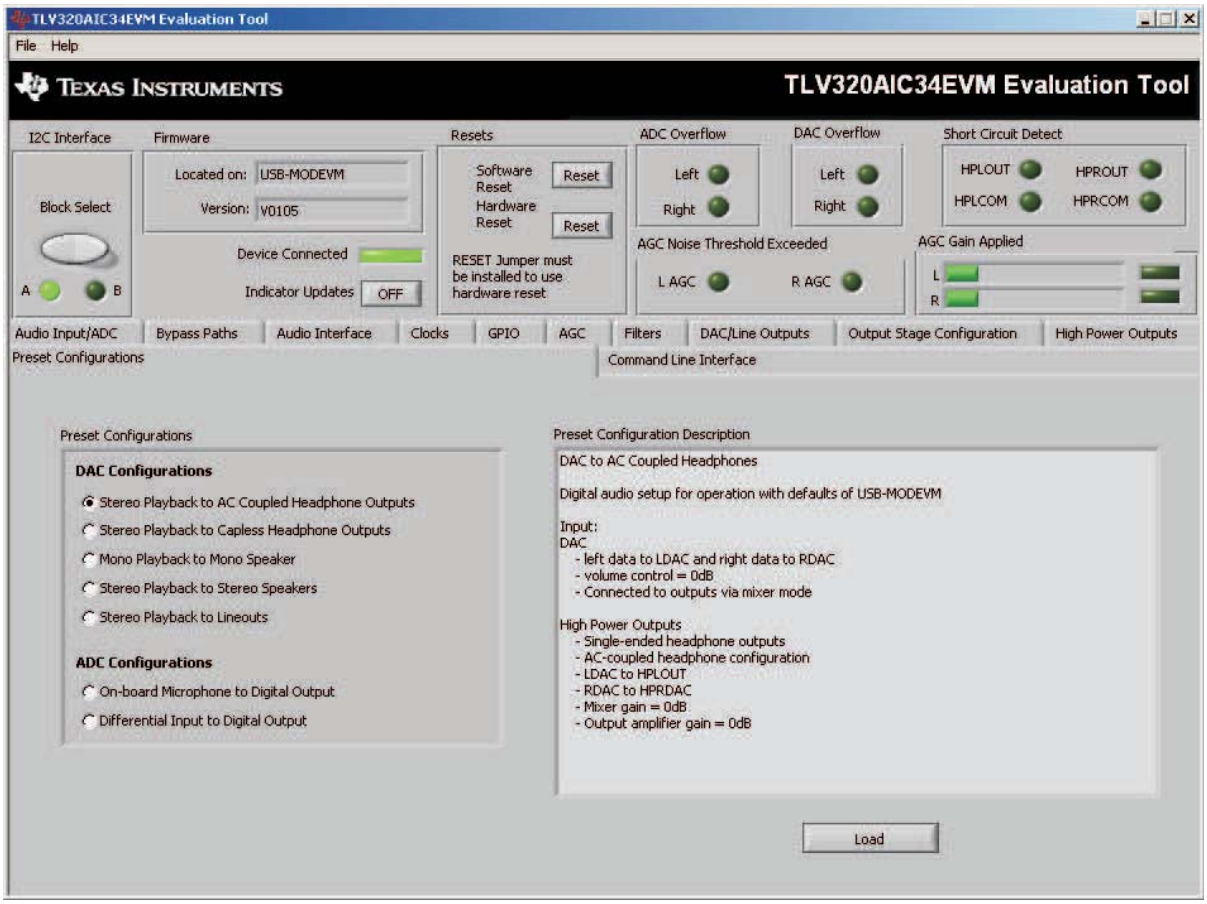


Figure 4. Default Configuration Tab

4.4 Audio Input/ADC Tab

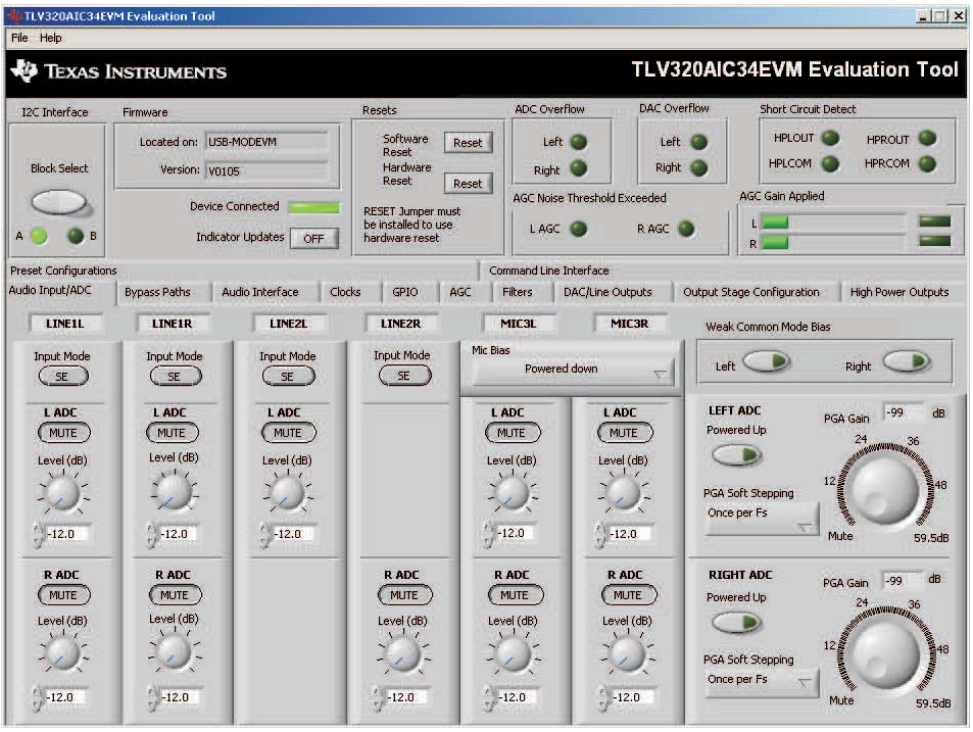


Figure 5. Audio Input Tab

The **Audio Input/ADC** Tab allows control of the analog input mixer and the ADC. The controls are displayed to look similar to an audio mixing console (see Figure 5). Each analog input channel has a vertical strip that corresponds to that channel. By default, all inputs are muted when the TLV320AIC34 is powered up.

To route an analog input to the ADC:

1. Select the **Input Mode** button to correctly show if the input signal is single-ended (*SE*) or fully-differential (*Diff*). Inputs that are single-ended should be made to the positive signal terminal.
2. Click on the button of the analog input channel that corresponds to the correct ADC. The caption of the button should change to *Active*. Note that the user can connect some channels to both ADCs, while others will only connect to one ADC.
3. Adjust the **Level** control to the desired attenuation for the connected channel. This level adjustment can be done independently for each connection.

The TLV320AIC34 offers a programmable microphone bias that can either be powered down or set to 2.0V, 2.5V, or the power supply voltage of the ADC (AVDD_ADC). Control of the microphone bias (mic bias) voltage is accomplished by using the **Mic Bias** pull-down menu button above the last two channel strips. To use the on-board microphone, JMP2 and JMP3 must be installed and nothing should be plugged into J6. In order for the mic bias settings in the software to take effect, JMP1 should be set to connect positions 2 and 3, so that MICBIAS_A is controlled by the TLV320AIC34. MICBIAS_B is available at J13-pin 14.

In the upper right portion of this tab are controls for **Weak Common Mode Bias**. Enabling these controls will result in unselected inputs to the ADC channels to be weakly biased to the ADC common mode voltage.

Below these controls are the controls for the ADC PGA, including the master volume controls for the ADC inputs. Each channel of the ADC can be powered up or down as needed using the **Powered Up** buttons. PGA soft-stepping for each channel is selected using the pull-down menu control. The two large knobs set the actual **ADC PGA Gain** and allow adjustment of the PGA gains from 0dB to 59.5dB in 0.5dB steps (excluding Mute). At the extreme counterclockwise rotation, the channel is muted. Rotating the knob clockwise increases the PGA gain, which is displayed in the box directly above the volume control.

4.5 Audio Interface Tab

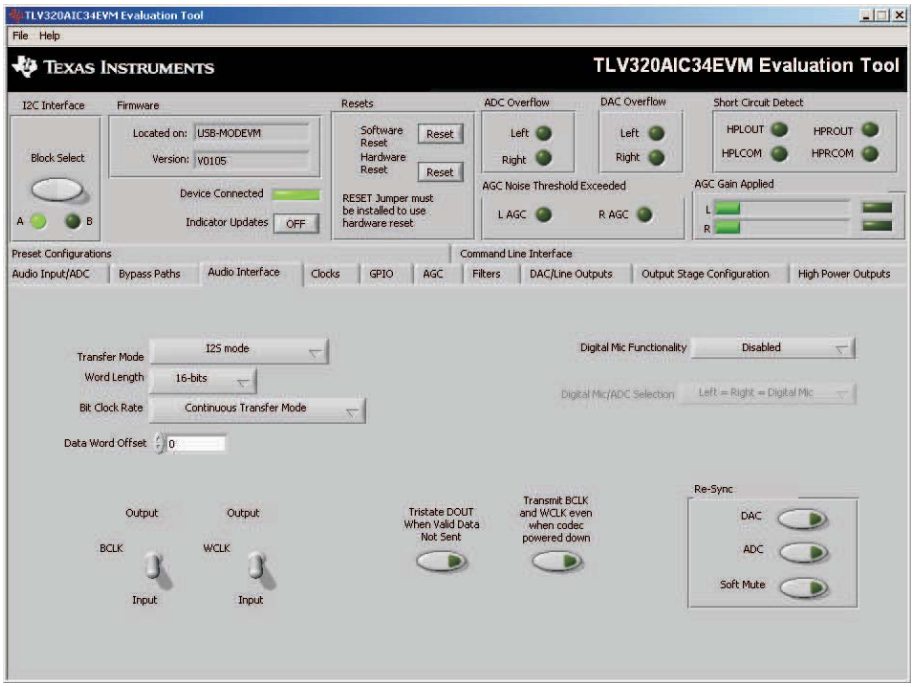


Figure 6. Audio Interface Tab

The Audio Interface tab (Figure 6) allows configuration of the audio digital data interface to the TLV320AIC34.

The interface mode may be selected using the **Transfer Mode** control—selecting either I^2S mode, DSP mode, or Right- or Left-Justified modes. Word length can be selected using the **Word Length** control, and the bit clock rate can also be selected using the **Bit Clock** rate control. The **Data Word Offset**, used in TDM mode (see the product data sheet) can also be selected on this tab.

Along the bottom of this tab are controls for choosing the **BLCK** and **WCLK** as being either inputs or outputs. With the codec configured in *Slave* mode, both the BCLK and WCLK are set to inputs. If the codec is in *Master* mode, then BCLK and WCLK are configured as outputs. Additionally, two buttons provide the options for 3-stating the DOUT line when there is not valid data and transmitting BLCK and WCLK when the codec is powered down.

Re-sync of the audio bus is enabled using the controls in the lower right corner of this screen. Re-sync is done if the group delay changes by more than ±FS/4 for the ADC or DAC sample rates (see the TLV320AIC34 data sheet). The channels can be soft muted when doing the re-sync if the **Soft Mute** button is enabled.

In the upper right corner of this tab is the **Digital Mic Functionality** control. The TLV320AIC34 can accept a data stream from a digital microphone, which would have its clock pin connected to the TLV320AIC34 GPIO1 pin, and the mic data connected to the GPIO2 pin. Once the digital microphone functionality is enabled, the **Digital Mic/ADC Selection** selection allows the user to choose if one or two digital microphones are connected to the codec. If only one digital microphone is connected, then the remaining ADC can be used with an analog input signal from the analog input pins. Refer to section Section 4.7 for a discussion of setting the GPIO pin options. The TLV320AIC34 can provide a modulator clock to the digital microphone with oversampling ratios (OSR) of 128, 64, or 32. For a detailed discussion of how to connect a digital microphone, refer to the application note *Using the Digital Microphone Function on TLV320AIC33EVM with AIC33EVM/USB-MODEVM System* (literature number SLAA275), available for download at www.ti.com.

The default mode for the EVM is configured as 44.1kHz, 16-bit, I^2 words, and the codec is a slave (BCLK and WCLK are supplied to the codec externally). For use with the PC software and the USB-MODEVM, the default settings should be used; no change to the software are required.

4.6 Clocks Tab

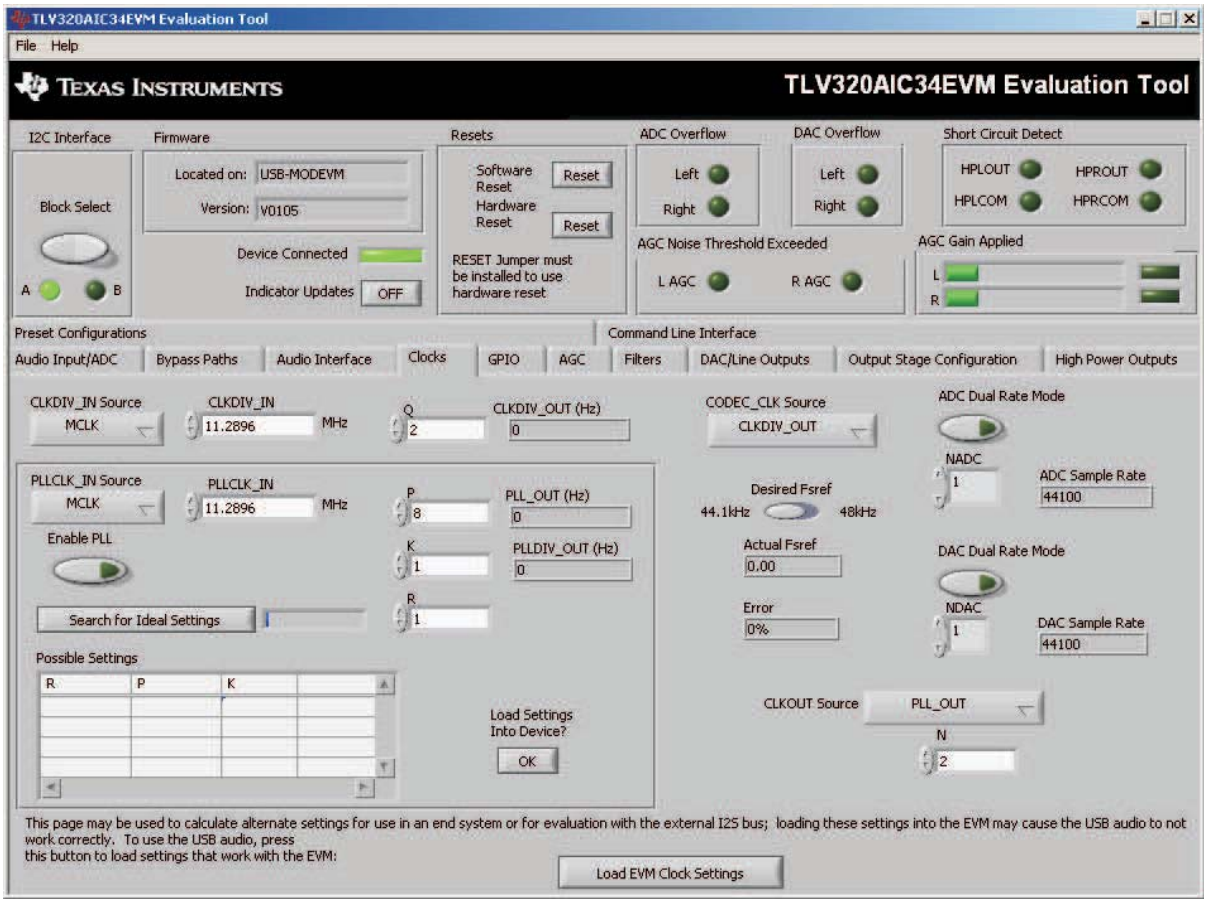


Figure 7. Clocks Tab

The TLV320AIC34 provides a phase-locked loop (PLL) that allows flexibility in the clock generation for the ADC and DAC sample rates. The Clocks tab contains the controls that can be used to configure the TLV320AIC34 for operation with a wide range of master clocks. See the Audio Clock Generation Processing figure in the TLV320AIC34 data sheet for further details of selecting the correct clock settings.

For use with the PC software and the USB-MODEVM, the clock settings must be set a certain way. If the settings are changed from the default settings which allow operation from the USB-MODEVM clock reference, the EVM settings can be restored automatically by pushing the **Load EVM Clock Settings** button at the bottom of this tab. Note that changing any of the clock settings from the values loaded when this button is pushed may result in the EVM not working properly with the PC software or USB interface. If an external audio bus is used (audio not driven over the USB bus), then settings may be changed to any valid combination. See Figure 7.

4.6.1 Configuring the codec clocks and Fsref calculation

The codec clock source is chosen by the **CODEC_CLK Source** control. When this control is set to *CLKDIV_OUT*, the PLL is not used; when set to *PLLDIV_OUT*, the PLL is used to generate the clocks.

Note: Per the TLV320AIC34 data sheet, the codec should be configured to allow the value of Fsref to fall between the values of 39kHz to 53kHz.

4.6.1.1 Use Without PLL

Setting up the TLV320AIC34 for clocking without using the PLL permits the lowest power consumption by the codec. The **CLKDIV_IN** source can be selected as either *MCLK*, *GPIO2*, or *BCLK*, the default is MCLK. The CLKDIV_IN frequency is then entered into the **CLKDIV_IN** box, in megahertz (MHz). The default value shown, 11.2896MHz, is the frequency used on the USB-MODEVM board. This value is then divided by the value of Q, which can be set from 2 to 17; the resulting *CLKDIV_OUT* frequency is shown in the indicator next to the **Q** control. The result frequency is shown as the *Actual Fsref*.

4.6.1.2 Use With The PLL

When PLLDIV_OUT is selected as the codec clock source, the PLL will be used. The PLL clock source is chosen using the **PLLCLK_IN** control, and may be set to either *MCLK*, *GPIO2*, or *BCLK*. The PLLCLK_IN frequency is then entered into the **PLLCLK_IN Source** box.

The *PLL_OUT* and *PLLDIV_OUT* indicators show the resulting PLL output frequencies with the values set for the P, K, and R parameters of the PLL. See the TLV320AIC34 data sheet for an explanation of these parameters. The parameters can be set by clicking on the up/down arrows of the **P**, **K**, and **R** combo boxes, or they can be typed into these boxes.

The values can also be calculated by the PC software. To use the PC software to find the ideal values of P, K, and R for a given PLL input frequency and desired Fsref:

1. Verify the correct reference frequency is entered into the **PLLCLK_IN Source** box in megaHertz (MHz)
2. The desired Fsref should be set using the **Fsref** switch.
3. Push the **Search for Ideal Settings** button. The software will start searching for ideal combinations of P, K, and R which achieve the desired Fsref. The possible settings for these parameters are displayed in the spreadsheet-like table labeled *Possible Settings*.
4. Click on a row in this table to select the P, K, and R values located in that row. Notice that when this is done, the software updates the P, K, R, PLL_OUT and PLLDIV_OUT readings, as well as the *Actual Fsref* and Error displays. The values show the calculations based on the values that were selected. This process does not actually load the values into the TLV320AIC34, however; it only updates the displays in the software. If more than one row exists, the user can choose the other rows to see which of the possible settings comes closest to the ideal settings.

When a suitable combination of P, K, and R have been chosen, pressing the **Load Settings into Device?** button will download these values into the appropriate registers on the TLV320AIC34.

4.6.1.3 Setting the ADC and DAC Sampling Rates

The Fsref frequency that is determine either enabling or bypassing the PLL (see Section 4.6.1.1 or Section 4.6.1.2) is used to determine the actual ADC and DAC sampling rates. Using the **NADC** and **NDAC** factors the sampling rates are derived from the Fsref. If dual rate mode is desired, this option can be enabled for either the ADC or DAC by pressing the corresponding **Dual Rate Mode** button. The ADC and DAC sampling rates are shown in the box to the right of each control.

4.7 GPIO Tab

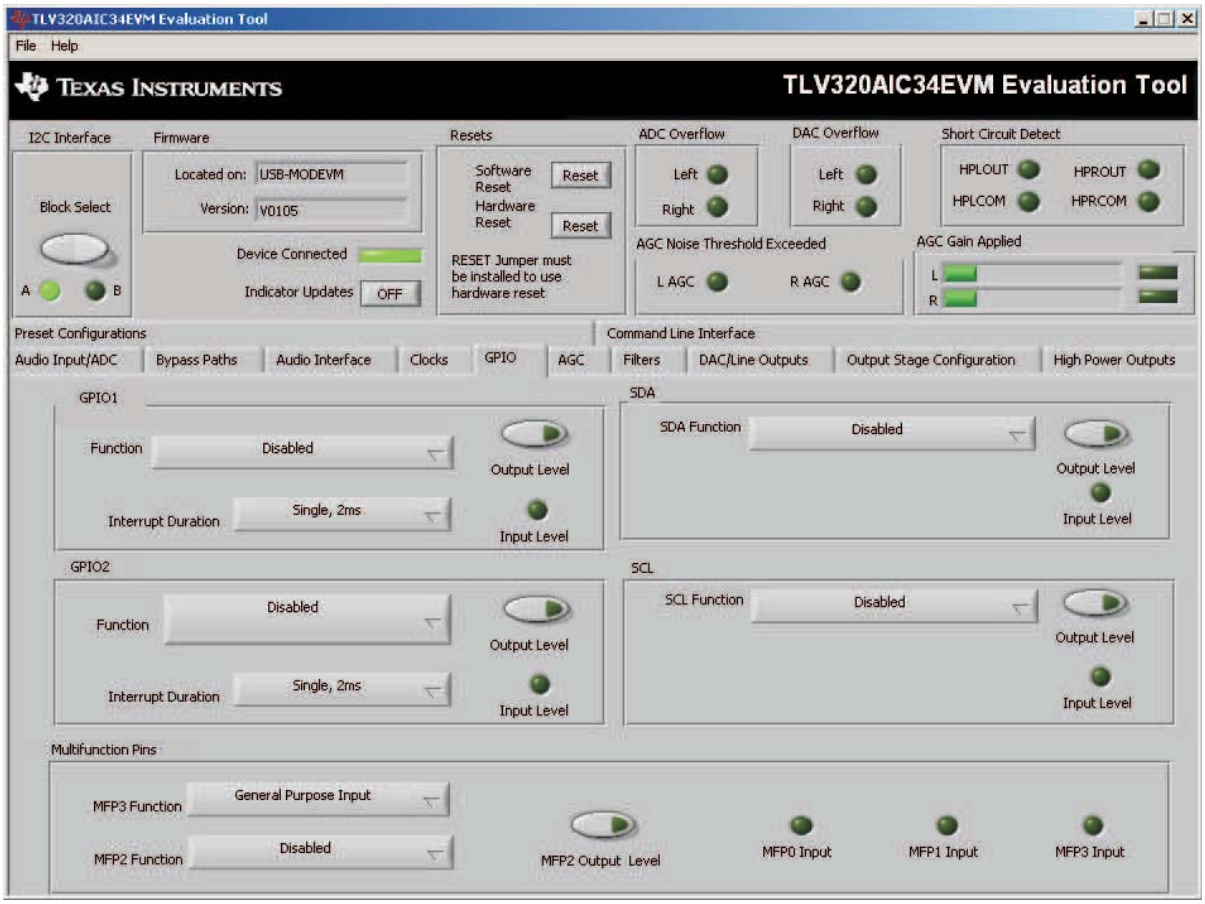


Figure 8. GPIO Tab

The GPIO tab (see Figure 8) selects options for the general-purpose inputs and outputs (GPIO) of the TLV320AIC34. Many pins on the TLV320AIC34 are denoted as *multifunction* pins, meaning they may be used for many different purposes.

The **GPIO1** groupbox contains controls for setting options for the GPIO1 pin. The **Function** control selects the function of GPIO1 from the following:

- ADC Word Clock
- An output clock derived from the reference clock (see TLV320AIC34 data sheet)
- Interrupt output pin to signal:
  - Short Circuit
  - AGC Noise Threshold detection
  - Jack/Headset detection
    - For use as an interrupt output, the behavior of the interrupt can be selected using the **Interrupt Duration** control. A *Single, 2ms* pulse can be delivered when the selected interrupt occurs, or *Continuous Pulses* can be generated signaling the interrupt.
- Alternate I^2S Word Clock
- A digital microphone output–modulator clock for use with a digital microphone (see Section 4.5 and the TLV320AIC34 data sheet).
- A general-purpose I/O pin
  - If selected as a *General Purpose Input*, the state of the GPIO1 pin is reflected by the **Input Level** indicator. If selected as a *General Purpose Output*, the state of the GPIO1 pin can be set by using the **Output Level** button.

In similar fashion, the GPIO2 pin can configured as the following using the **Function** control in the **GPIO2** groupbox.

- An alternate I^2S bus
- An interrupt output
- A general-purpose I/O pin
- A digital microphone input

The other controls in this groupbox work the same as the corresponding controls for GPIO1.

The control interface for the TLV320AIC34 is always selected to be I^2C so the **SDA** and **SCL** groupboxes and controls within them are disabled.

The **MFP3 Function** control selects MFP3 to be used either as a *General Purpose Input* or as the data input line for the alternate I^2S bus. The **MFP2 Function** control selects MFP2 as either *Disabled* or as a *General Purpose Output*. When used as an output, the **MFP2 Output Level** control sets the output state of the MFP2 pin either high or low. The states of the MFP0, MFP1 and MP3 inputs are indicated by the three indicator lights on the right-hand side of this groupbox.

4.8 AGC Tab

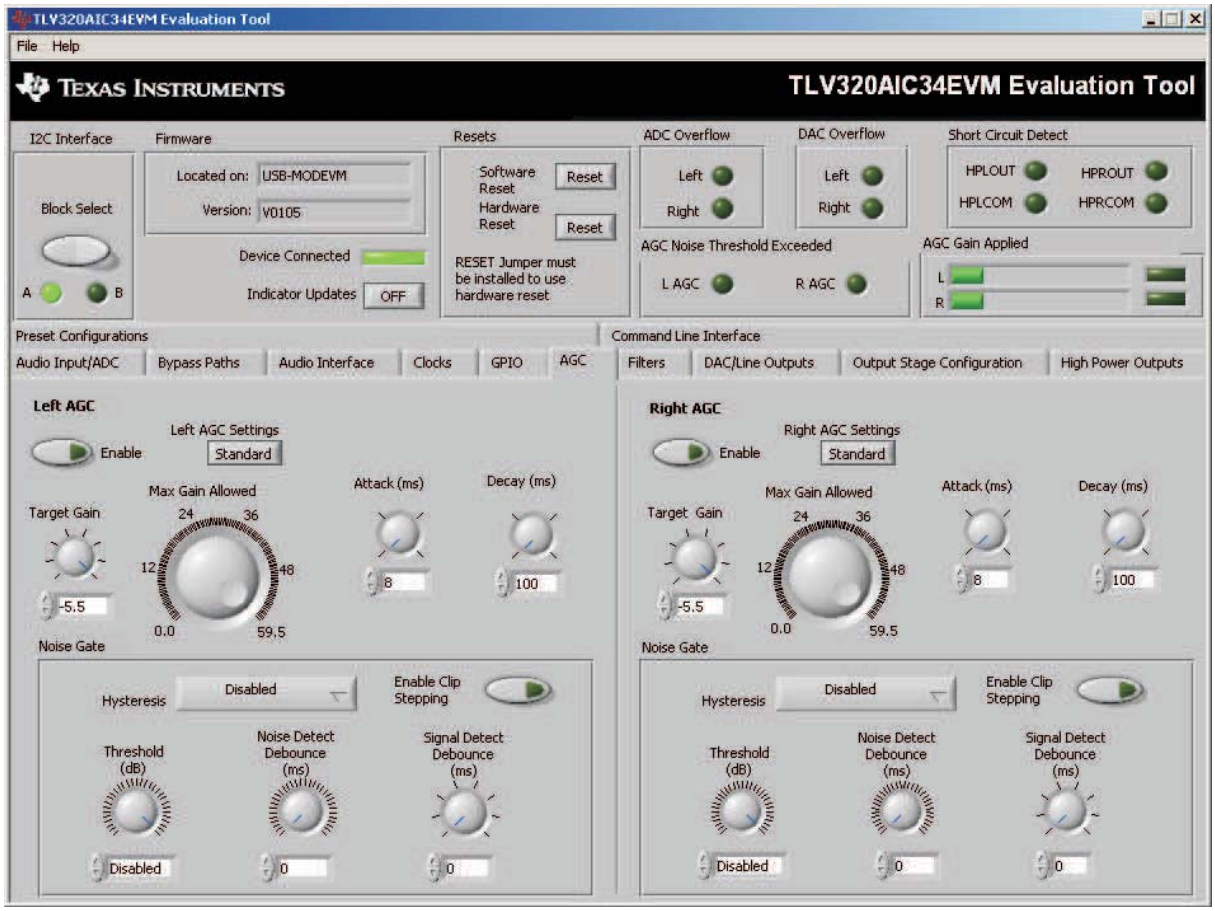


Figure 9. AGC Tab

The AGC tab (see Figure 9) consists of two identical sets of controls, one for the left channel and the other for the right channel. The AGC function is described in the TLV320AIC34 data sheet.

The AGC can be enabled for each channel using the **Enable AGC** button. **Target** gain, **Attack** time in milliseconds, **Decay** time in milliseconds, and the **Maximum PGA Gain Allowed** can all be set, respectively, using the four corresponding knobs in each channel.

The TLV320AIC34 allows for the Attack and Decay times of the AGC to be setup in two different modes, standard and advanced. The **Left/Right AGC Settings** button determines the mode selection. The *Standard*mode provides several preset times that can be selected by adjustments made to the **Attack**and **Decay**knobs. If finer control over the times is required, then the *Advanced* mode is selected to change to the settings. When the *Advanced* mode is enabled, two tabs should appear that allow separate, advanced control of the Attack and Delay times of the AGC (see Figure 10 and Figure 11). These options allow selection of the base time as well as a multiplier to achieve the actual times shown in the corresponding text box. The **Use advanced settings?** button should be enabled to program the registers with the correct values selected via the pull-down options for base time and multiplier.



Figure 10. Left AGC Settings

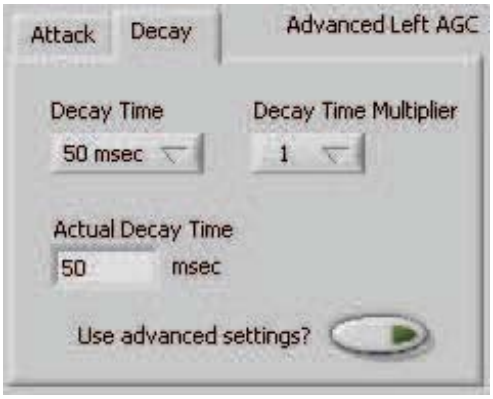


Figure 11. Advanced

Noise gate functions, such as **Hysteresis**, **Enable Clip stepping**, **Threshold (dB)**, **Signal Detect Debounce (ms)**, and **Noise Detect Debounce (ms)** are set using the corresponding controls in the **Noise Gate** groupbox for each channel.

4.9 Filters Tab

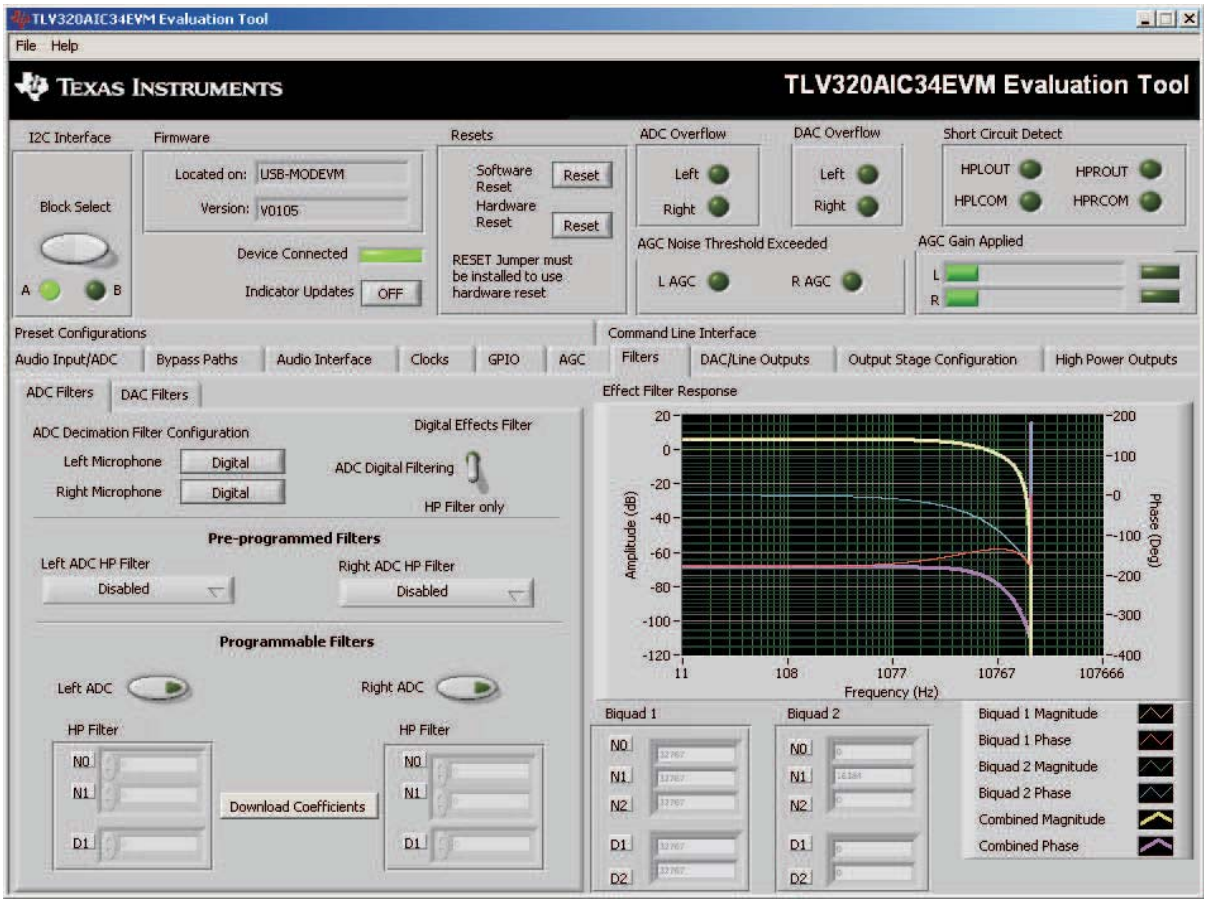


Figure 12. Filters Tab

The TLV320AIC34 has an advanced feature set for applying digital filtering to audio signals. This tab controls all of the filter features of the TLV320AIC34. In order to use this tab and have plotting of filter responses correct, the DAC sample rate must be set correctly. Therefore, the clocks must be set up correctly in the software following the discussion in Section 4.6. See Figure 12.

The AIC34 digital filtering is available to both the ADC and DAC. The ADC has optional high pass filtering and allows the digital output from the ADC through digital effects filtering before exiting the codec through the PCM interface. Likewise, the digital audio data can be routed through the digital effects filtering before passing through the optional de-emphasis filter before the DAC. The digital effects filtering can only be connected to either the ADC or DAC, not both at the same time.

The Figure 12 is divided into several areas. The left side of the tab, is used to select between the DAC or ADC filters and assist in the selection and calculating the desired filter coefficients. The right hand side of the tab shows a frequency response plot of the digital effects filter selected and the coefficients that are programmed into the device. The plots show the magnitude and phase response of each biquad section, plus the combined responses of the two biquad filters. Note that the plot shows only the responses of the effect filters, not the combined response of those filter along with the de-emphasis and ADC high-pass filters.

4.9.1 ADC Filters

4.9.1.1 High Pass Filter

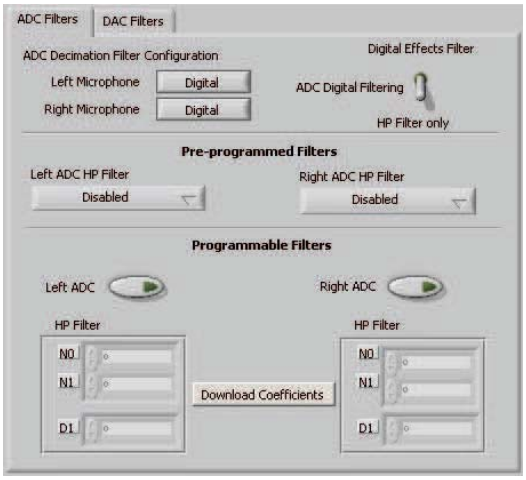


Figure 13. ADC High Pass Filters

The TLV320AIC34 ADC provides the option of enabling a high-pass filter, which helps to reduce the effects of DC offsets in the system. The Figure 13 tab shows the options for programming various filter associated with the ADC. The high-pass filter has two modes: standard and programmable.

The standard high-pass filter option (Figure 14) allows for the selection of the high-pass filter frequency from several preset options that can be chosen with the **Left ADC HP Filter** and **Right ADC HP Filter** controls. The four options for this setting are disabled, or three different corner frequencies which are based on the ADC sample rate.

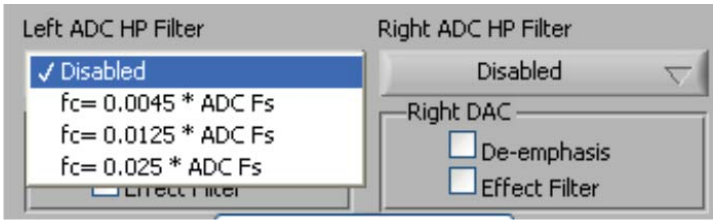


Figure 14. ADC Highpass Filter Settings

For custom filter requirements, the programmable function allows custom coefficients to achieve a different filter than provided by the preset filters. The controls for the programmable high-pass filter are located under the **Programmable Filters** heading. The process should following the following steps:

1. Enter The filter coefficients can be entered in the **HP Filter** controls near the bottom of the tab.
2. Press the **Download Coefficients** button to download the coefficients to the codec registers.
3. Enable the Programmable High-Pass Filters by selecting the **Left ADC** and **Right ADC** buttons.

The programmable high-pass filter should now be correctly programmed and enabled. The ADC can now be enabled with the high-pass filter.

4.9.1.2 Digital Effects Filter - ADC

The ADC digital outputs stream can be routed through the digital effects filter in the codec to allow custom audio performance. The digital effects filter cannot operate on both the ADC or DAC at the same time. The digital effects filter operation is discussed in Section 4.9.3

4.9.2 DAC Filters

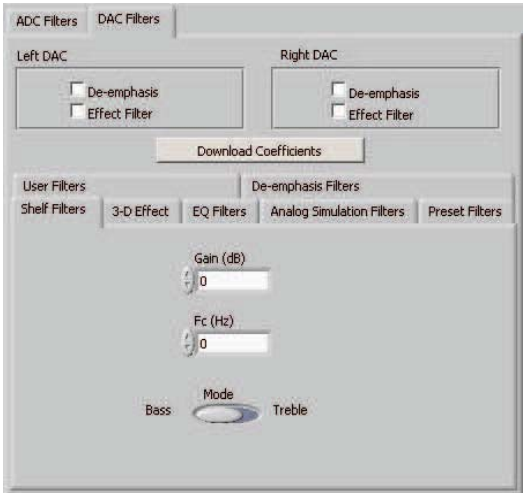


Figure 15. DAC Filters

4.9.2.1 De-emphasis Filters

The de-emphasis filters used in the TLV320AIC34 can be programmed as described in the TLV320AIC34 data sheet, using this tab (Figure 16). Enter the coefficients for the de-emphasis filter response desired. While on this tab, the de-emphasis response will be shown on the *Effect Filter Response* graph; however, note that this response is not included in graphs of other effect responses when on the other filter design tabs.

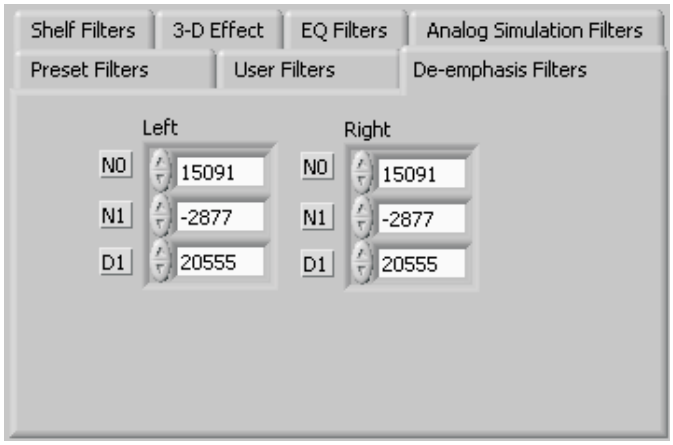


Figure 16. De-emphasis Filters

4.9.2.2 DAC Digital Effects Filter

The digital audio input stream can be routed through the digital effects filter in the codec before routing to the DAC to allow custom audio performance. The digital effects filter cannot operate on both the ADC or DAC at the same time. The digital effects filter operation is discussed in Section 4.9.3

4.9.3 Digital Effects Filters

The digital effect filters (the biquad filters) of the TLV320AIC34 are selected using the checkboxes shown in Figure 17. The De-emphasis filters are described in the TLV320AIC34 data sheet, and their coefficients may be changed (see Figure 15).

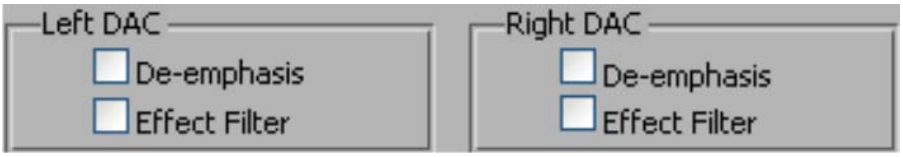


Figure 17. Enabling Filters

When designing filters for use with TLV320AIC34, the software allows for several different filter types to be used. These options are shown on a tab control in the lower left corner of the screen. When a filter type is selected, and suitable input parameters defined, the response will be shown in the *Effect Filter Response* graph. Regardless of the setting for enabling the Effect Filter, the filter coefficients are not loaded into the TLV320AIC34 until the **Download Coefficients** button is pressed. To avoid noise during the update of coefficients, it is recommended that the user uncheck the **Effect Filter enable** checkboxes before downloading coefficients. Once the desired coefficients are in the TLV320AIC34, enable the Effect Filters by checking the boxes again.

4.9.3.1 Shelf Filters

A shelf filter is a simple filter that applies a gain (positive or negative) to frequencies above or below a certain corner frequency. As shown in Figure 18, in *Bass* mode a shelf filter applies a gain to frequencies below the corner frequency; in *Treble* mode the gain is applied to frequencies above the corner frequency.

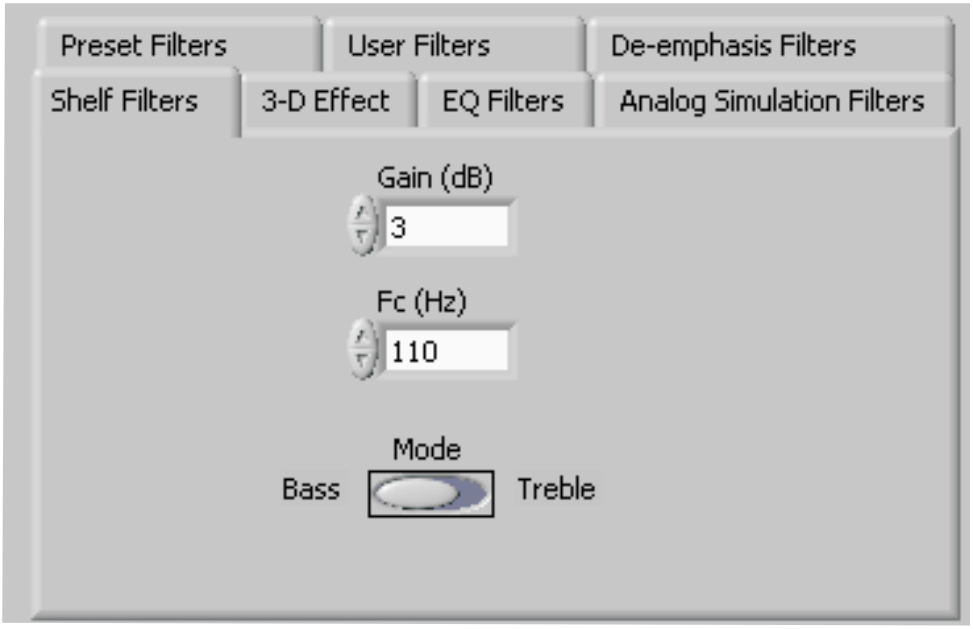


Figure 18. Shelf Filters

To use these filters, enter the gain desired and the corner frequency. Choose the mode to use (*Bass* or *Treble*); the response will be plotted on the *Effect Filter Response* graph.

4.9.3.2 EQ Filters

EQ, or parametric, filters can be designed on this tab (see Figure 19). Enter a gain, bandwidth, and a center frequency (Fc). Either bandpass (positive gain) or band-reject (negative gain) filters can be created

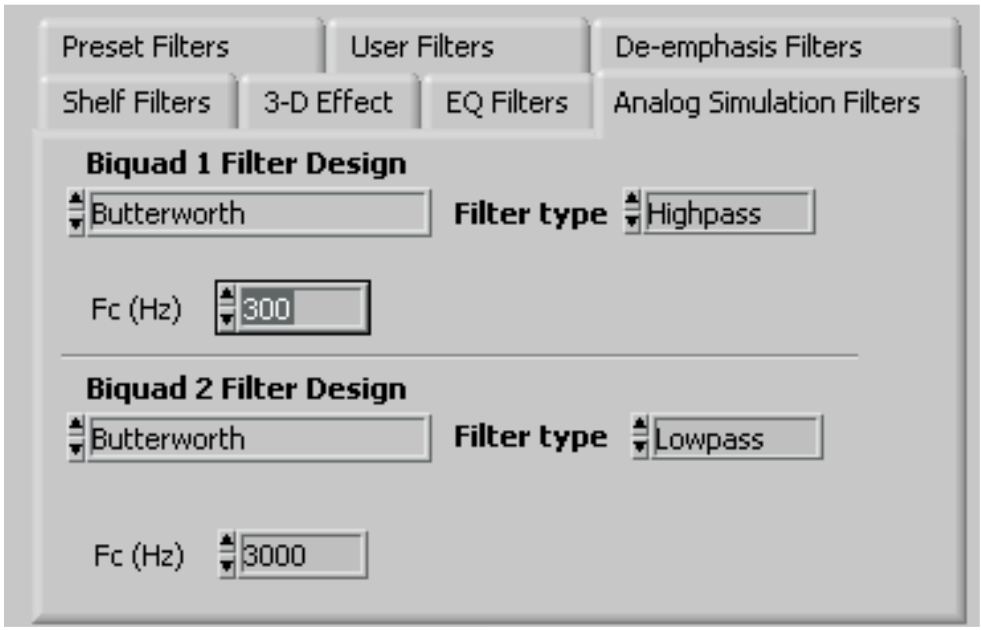


Figure 19. EQ Filters

4.9.3.3 Analog Simulation Filters

Biquads are quite good at simulating analog filter designs. For each biquad section on this tab, enter the desired analog filter type to simulate (Butterworth, Chebyshev, Inverse Chebyshev, Elliptic or Bessel). Parameter entry boxes appropriate to the filter type will be shown (ripple, for example, with Chebyshev filters, etc.). Enter the desired design parameters and the response will be shown. (See Figure 20.)

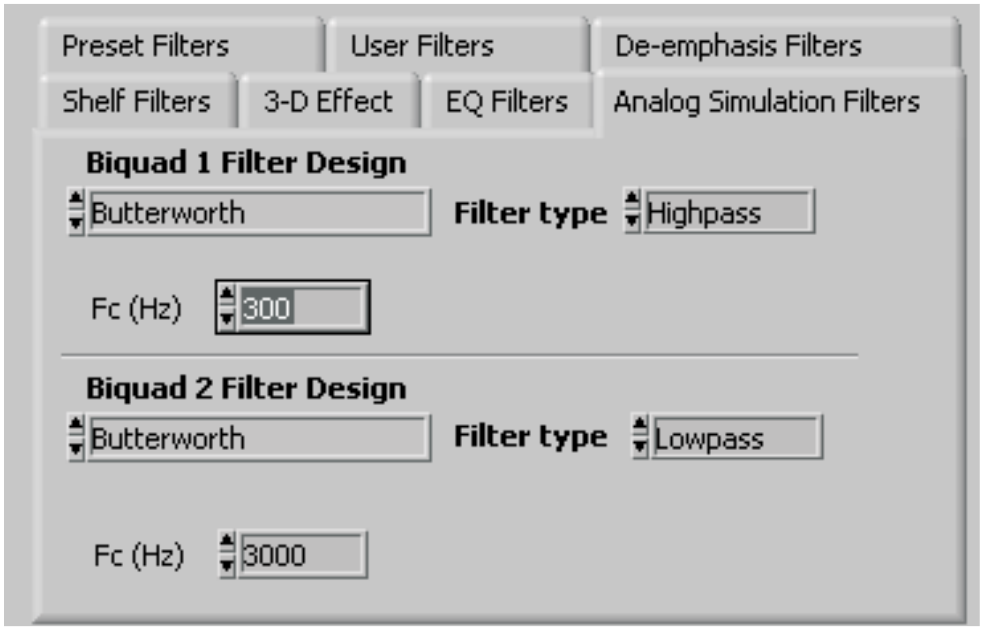


Figure 20. Analog Simulation Filters

4.9.3.4 Preset Filters

Many applications are designed to provide preset filters common for certain types of program material. This tab (see Figure 21) allows selection of one of four preset filter responses - Rock, Jazz, Classical, or Pop.

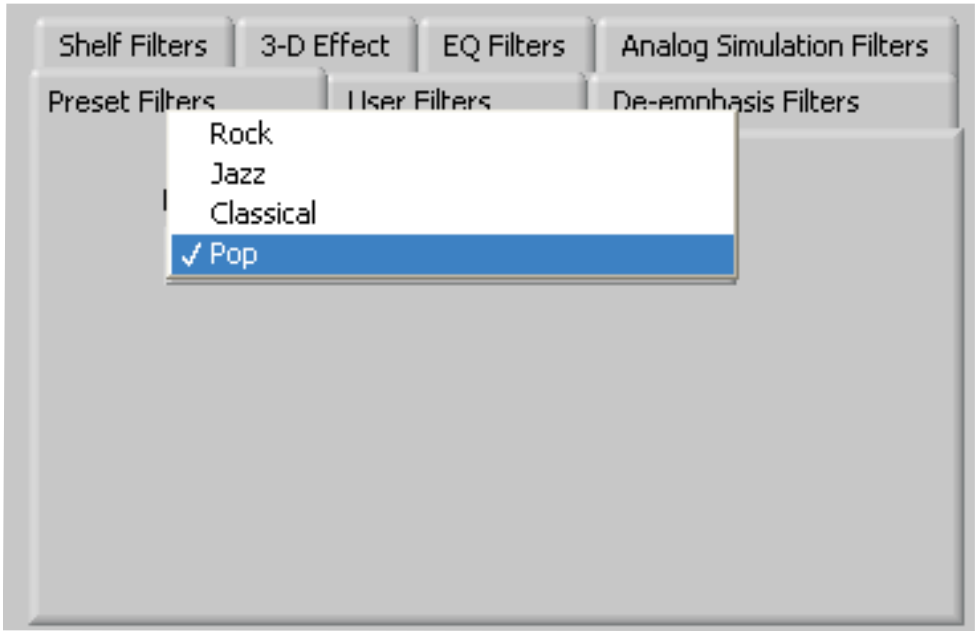


Figure 21. Preset Filters

4.9.3.5 User Filters

If filter coefficients are known, they can be entered directly on this tab (see Figure 22) for both biquads for both left and right channels. The filter response will ***not*** be shown on the *Effect Filter Response* graph for user filters.

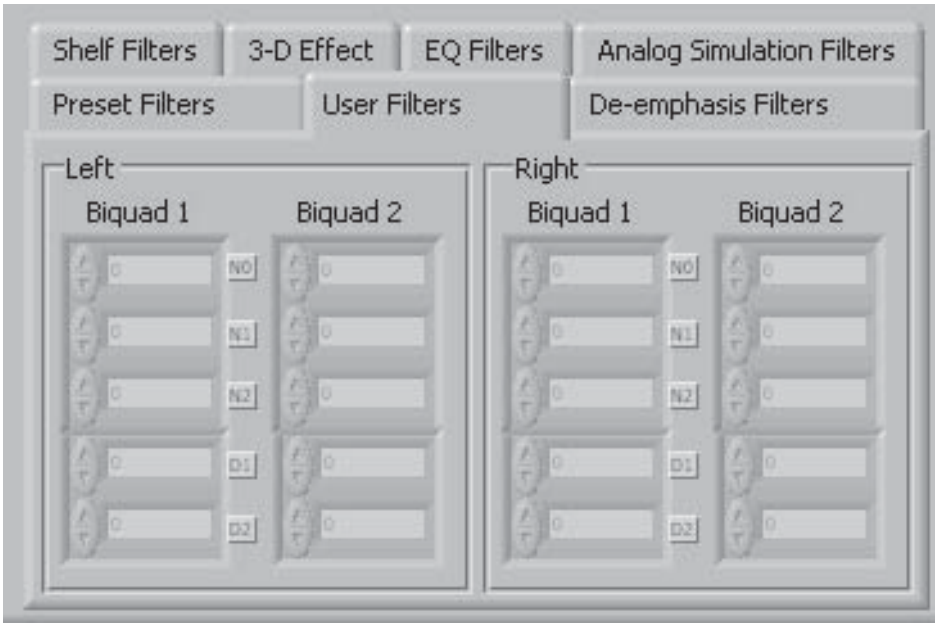


Figure 22. User Filters

4.9.3.6 3D Effect

The 3D effect is described in the TLV320AIC34 data sheet. It uses the two biquad sections differently than most other effect filter settings. To use this effect properly, make sure the appropriate coefficients are already loaded into the two biquad sections. The User Filters tab may be used to load the coefficients. See Figure 23.

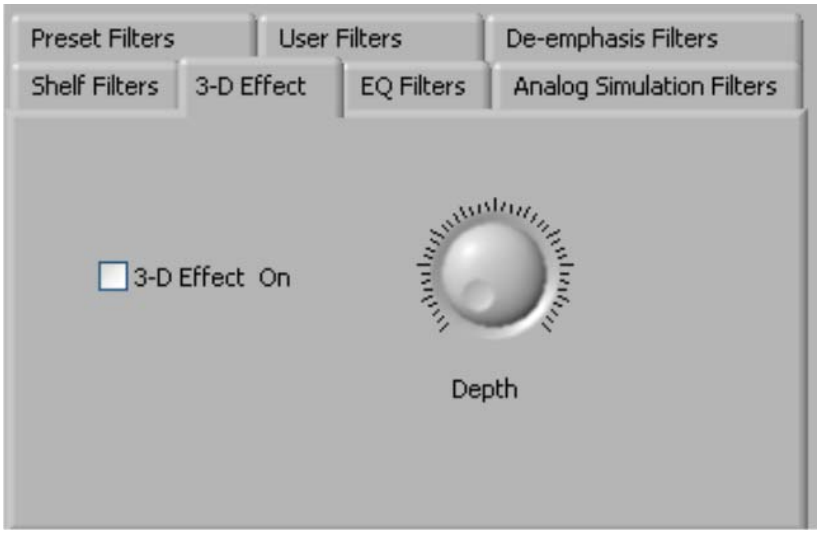


Figure 23. 3D Effect Settings

To enable the 3D effect, check the **3D Effect On** box. The **Depth** knob controls the value of the 3D Attenuation Coefficient.

4.10 Output Stage Configuration Tab

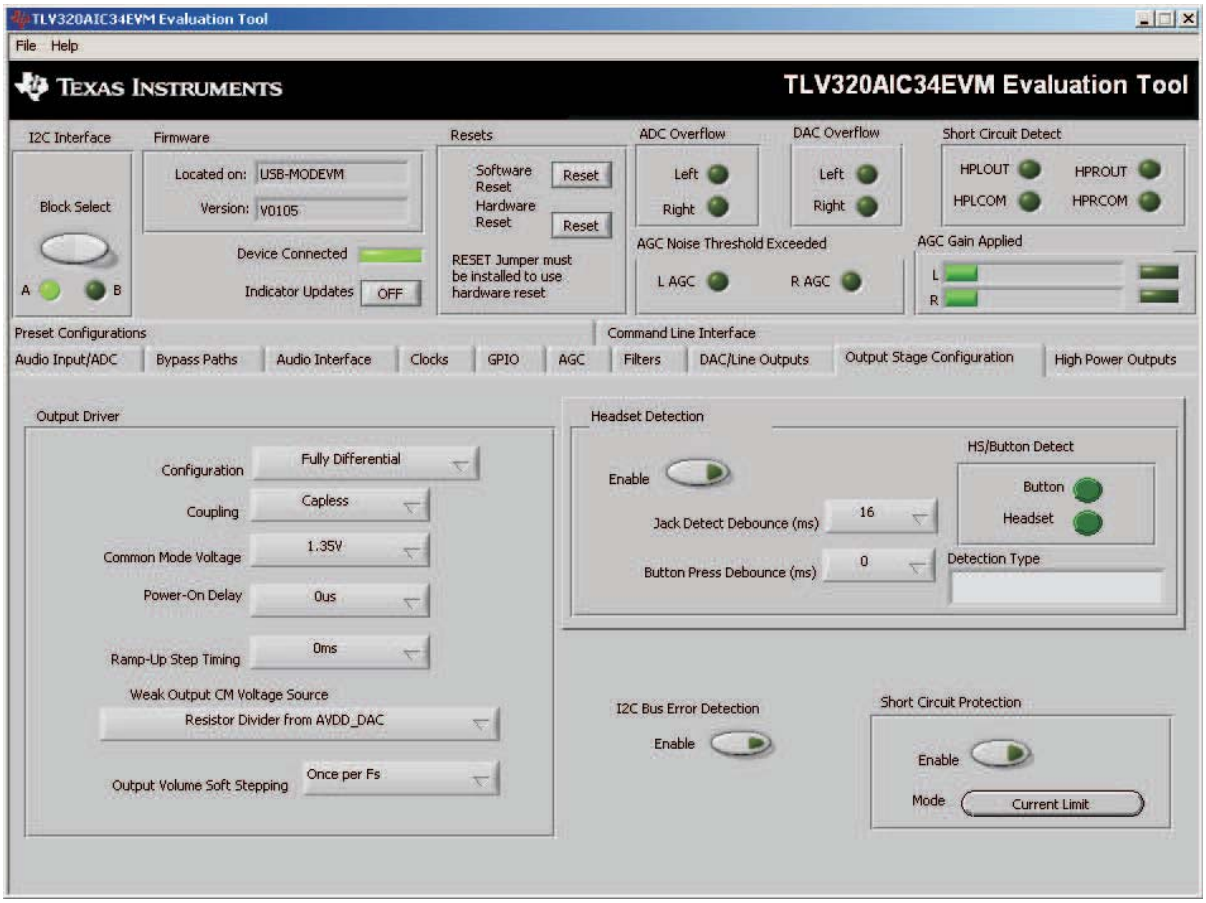


Figure 24. Output Stage Configuration Tab

The Output Stage Configuration tab (Figure 24) allows for setting various features of the output drivers.

The **Configuration** control may be set as either *Fully-Differential* or *Pseudo-Differential*. This control is used to determine if the output stage is being used to drive a fully differential output load or a output load where one of the outputs if referenced to a common-mode voltage (pseudo-differential).

The output **Coupling** control can be chosen as either *Capless* or *AC-coupled*. This setting should correspond to the setting of the hardware switch (SW1) on the TLV320AIC34EVM.

The common mode voltage of the outputs may be set to 1.35V, 1.5V, 1.65V, or 1.8V using the **Common Mode Voltage** control.

The TLV320AIC34 offers several options to help reduce the turn-on/off pop of the output amplifiers. The **Power-On Delay** of the output drivers can be set using the corresponding control from 0's up to 4 seconds. **Ramp-Up Step Timing** can also be adjusted from 0ms to 4ms. The outputs can be set to soft-step their volume changes, using the **Output Volume Soft Stepping** control, and set to step once per Fs period, once per two Fs periods, or soft-stepping can be disabled altogether.

The high power outputs of the TLV320AIC34 can be configured to go to a weak common-mode voltage when powered down. The source of this weak common-mode voltage can be set on this tab with the **Weak Output CM Voltage Source** drop-down. Choices for the source are either a resistor divider off the AVDD_DAC supply, or a bandgap reference. See the data sheet for more details on this option.

Headset detection features are enabled using the **Enable** button in the **Headset Detection** groupbox. When enabled, the indicators in the **HS/Button Detect** groupbox will light when either a button press or headset is detected. When a headset is detected, the type of headset is displayed in the **Detection Type** indicator. Debounce times for detection are set using the **Jack Detect Debounce** and **Button Press Debounce** controls, which offer debounce times in varying numbers of milliseconds. See the TLV320AIC34 data sheet for a discussion of headset detection.

Output short-circuit protection can be enabled in the **Short Circuit Protection** groupbox. Short Circuit Protection can use a current-limit mode, where the drivers will limit current output if a short-circuit condition is detected, or in a mode where the drivers will power down when such a condition exists.

The **I^2C Bus Error Detection** button allows the user to enable circuitry which will set a register bit (Register 107, D0) if an I^2C bus error is detected.

4.11 DAC/Line Outputs Tab

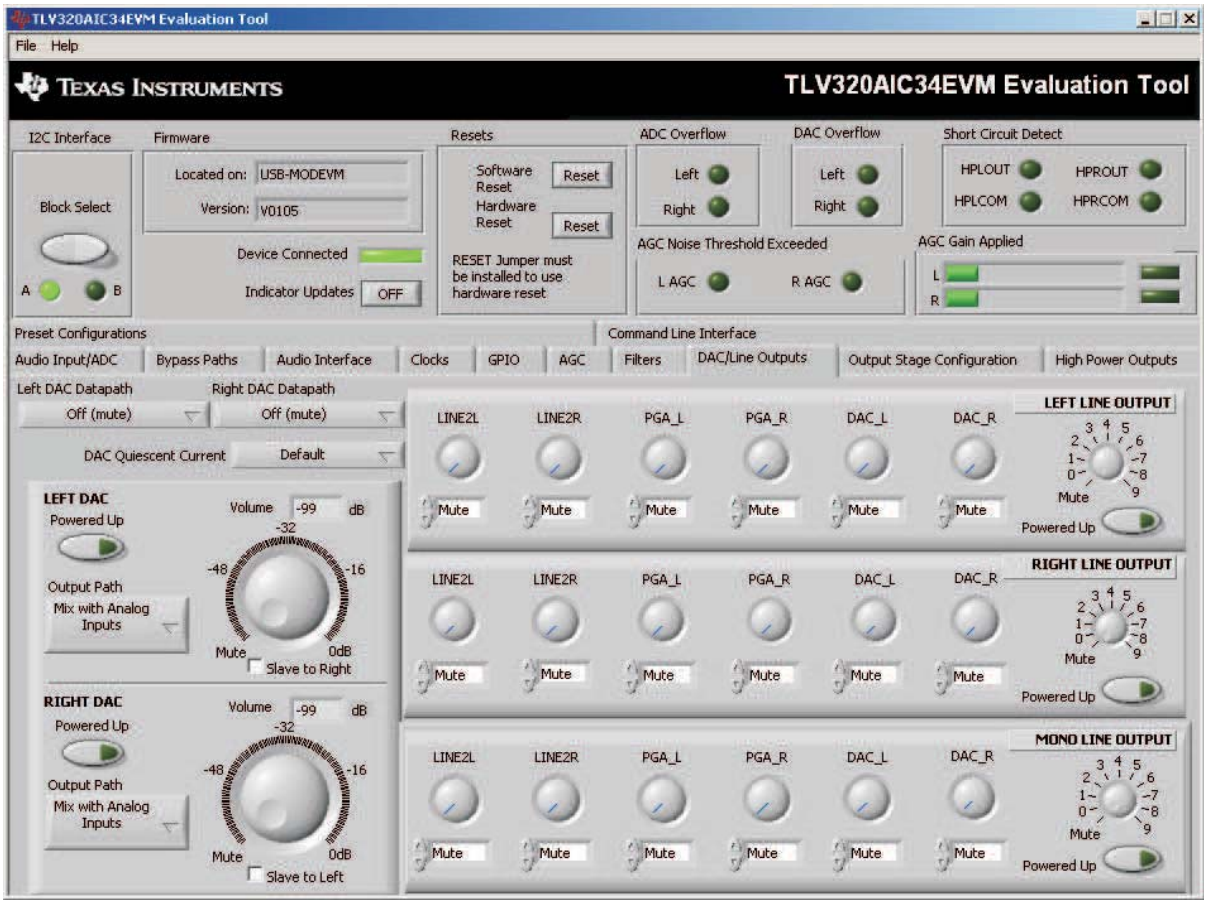


Figure 25. DAC/Line Outputs Tab

The DAC/Line Outputs tab controls the DAC power and volume, as well as routing of digital data to the DACs and the analog line output from the DACs. (See Figure 25.)

4.11.1 DAC Controls

On the left side of this tab are controls for the left and right DACs.

In similar fashion as the ADC, the DAC controls are set up to allow powering of each DAC individually, and setting the output level. Each channel's level can be set independently using the corresponding **Volume** knob. Alternately, by checking the **Slave to Right** box, the left channel Volume can be made to track the right channel Volume knob setting; checking the **Slave to Left** box causes the right channel Volume knob to track the left Volume knob setting.

Data going to the DACs is selected using the drop-down boxes under the **Left** and **Right DAC Datapath**. Each DAC channel can be selected to be off, use left channel data, use right channel data, or use a mono mix of the left and right data.

Analog audio coming from the DACs is routed to outputs using the **Output Path** controls in each DAC control panel. The DAC output can be mixed with the analog inputs (LINE2L, LINE2R, PGA_L, PGA_R) and routed to the Line or High Power outputs using the mixer controls for these outputs on this tab (for the line outputs) or on the High Power Outputs tab (for the high power outputs). If the DAC is to be routed directly to either the Line or HP outputs, these can be selected as choices in the **Output Path** control. Note that if the Line or HP outputs are selected as the Output Path, the mixer controls on this tab and the High Power Output tabs have no effect.

4.11.2 Line Output Mixers

On the right side of this tab are horizontal panels where the analog output mixing functions for the line outputs are located.

Each line output master volume is controlled by the knob at the far right of these panels, below the line output labels. The output amplifier gain can be muted or set at a value between 0 and 9dB in 1 dB steps. Power/Enabled status for the line output can also be controlled using the button below this master output knob (**Powered Up**).

If the DAC **Output Path** control is set to *Mix with Analog Inputs*, the six knobs in each panel can be used to set the individual level of signals routed and mixed to the line output. LINE2L, LINE2R, PGA_L, PGA_R, and DAC_L and DAC_R levels can each be set to create a custom mix of signals presented to that particular line output. **Note:** if the DAC **Output Path** control is set to anything other than *Mix with Analog Inputs*, these controls have no effect.

4.12 High Power Outputs Tab

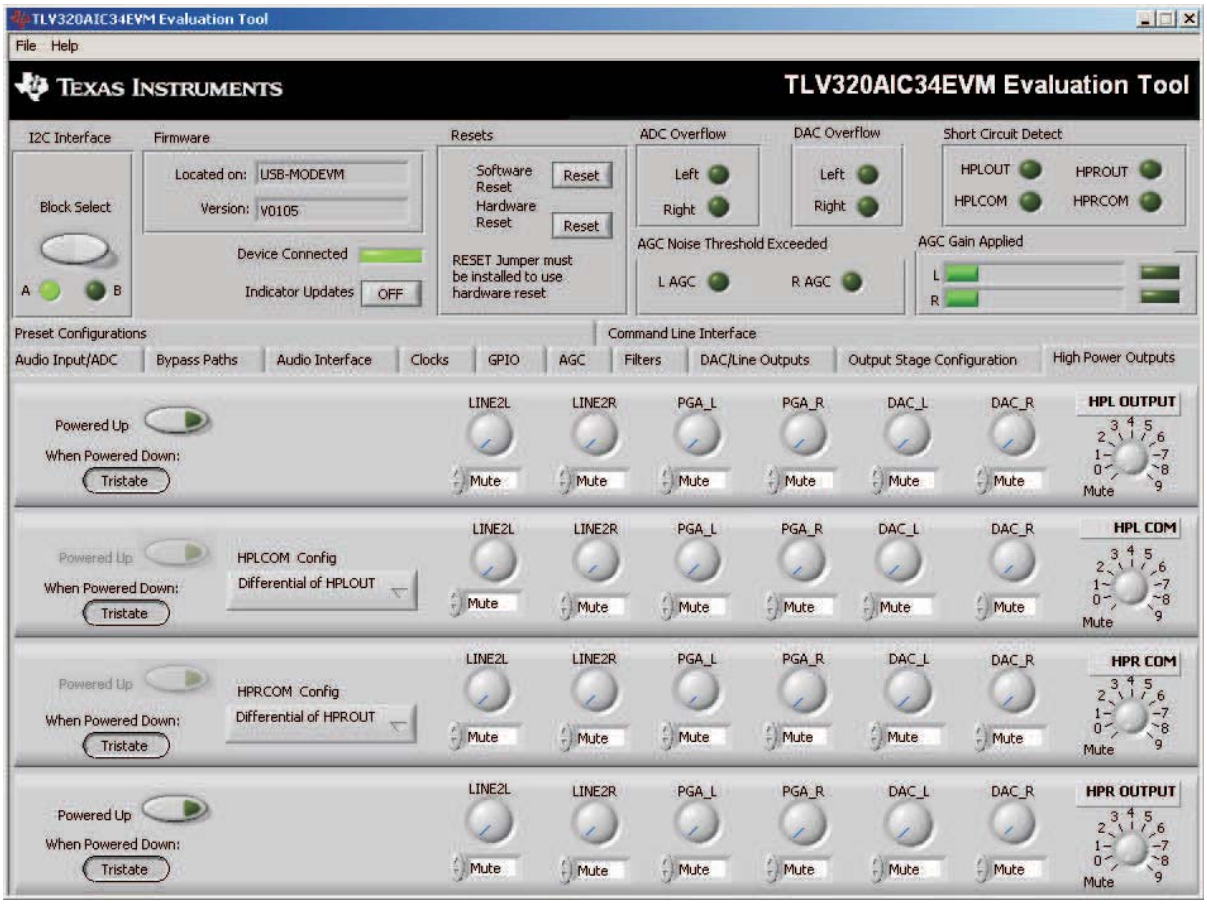


Figure 26. High Power Outputs Tab

This tab contains four horizontal groupings of controls, one for each of the high power outputs. Each output has a mixer to mix the LINE2L, LINE2R, PGA_L, PGA_R, DAC_L and DAC_R signals, assuming that the DACs are not routed directly to the high power outputs (see Section 4.11).

At the left of each output strip is a **Powered Up** button that controls whether the corresponding output is powered up or not. The **When powered down** button allows the outputs to be tri-stated or driven weakly to a the output common mode voltage.

The **HPxCOM** outputs (*HPLCOM* and *HPRCOM*) can be used as independent output channels or can be used as complementary signals to the HPLOUT and HPROUT outputs. In these complementary configurations, the **HPxCOM** outputs can be selected as *Differential of HPxOUT* signals to the corresponding outputs or may be set to be a common mode voltage (*Constant VCM Out*. When used in these configurations, the **Powered Up** button for the **HPxCOM** output is disabled, as the power mode for that output will track the power status of the HPL or HPR output that the COM output is tracking.

The **HPRCOM Config** selector allows a couple additional options compared to the **HPLCOM Config** selector. *Differential of HPLCOM* allows the HPRCOM to be the complementary signal of HPLCOM for driving a differential load between the **HPxCOM** outputs. The selector also allows *Ext. Feedback/HPLCOM constant VCM* as an option. This option is used when the high power outputs are configured for *Capless* output drive, where HPLCOM is configured as *Constant VCM Out*. The feedback option provides feedback to the output and lowers the output impedance of HPLCOM.

At the right side of the output strip is a master volume knob for that output, which allows the output amplifier gain to be muted or set from 0 to 9dB in 1dB.

4.13 Command Line Interface Tab

A simple scripting language controls the TAS1020 on the USB-MODEVM from the LabView™-based PC software. The main program controls, described previously, do nothing more than write a script which is then handed off to an interpreter that sends the appropriate data to the correct USB endpoint. Because this system is script-based, provision is made in this tab for the user to view the scripting commands created as the controls are manipulated, as well as load and execute other scripts that have been written and saved (see Figure 27). This design allows the software to be used as a quick test tool or to help provide troubleshooting information in the rare event that the user encounters problem with this EVM.

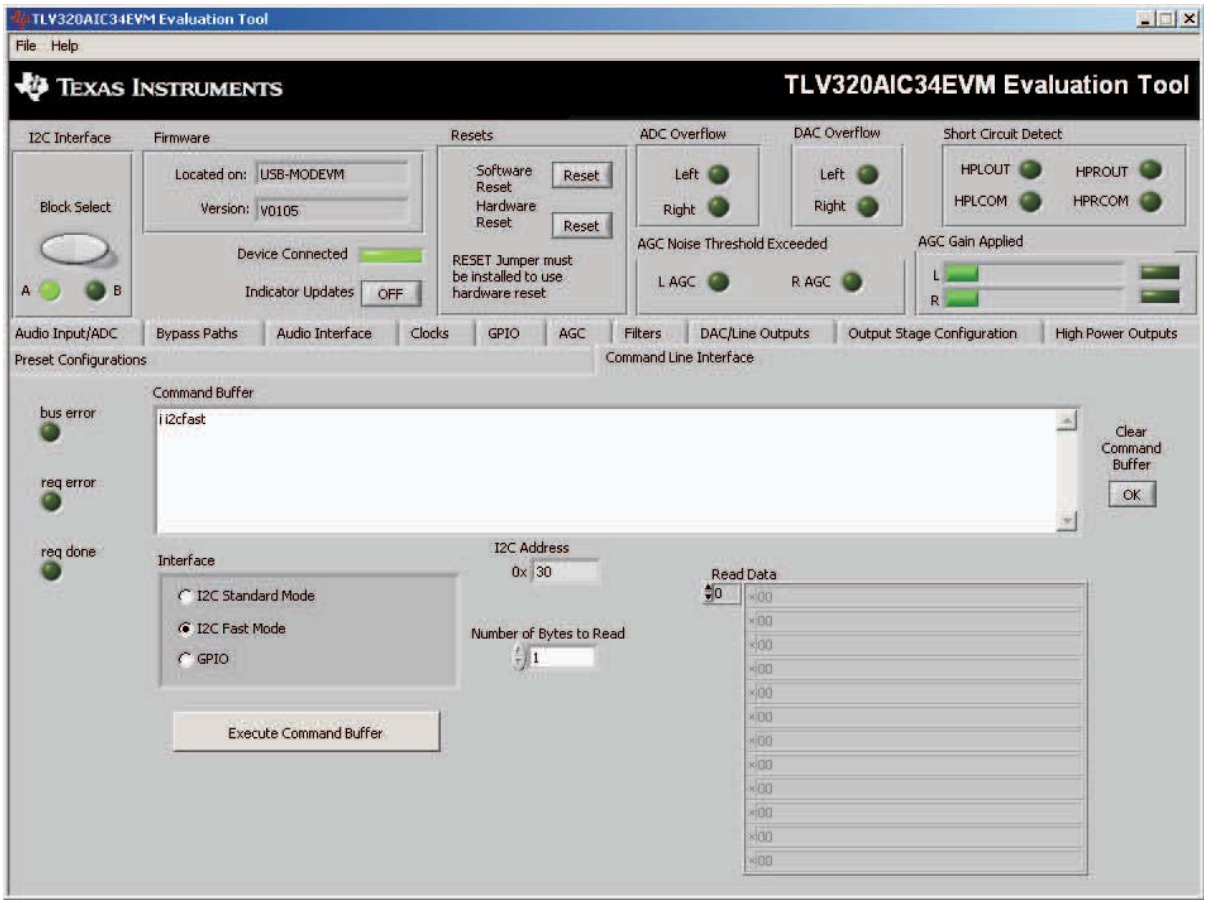


Figure 27. Command Line Interface Tab

A script is loaded into the command buffer, either by operating the controls on the other tabs or by loading a script file. When executed, the return packets of data which result from each command will be displayed in the **Read Data** array control. When executing several commands, the Read Data control shows only the results of the last command. To see the results after every executed command, use the logging function described below.

The File menu (Figure 28) provides some options for working with scripts. The first option, *Open Command File...*, loads a command file script into the command buffer. This script can then be executed by pressing the **Execute Command Buffer** button.

The second option is *Log Script and Results...*, which opens a file save dialog box. Choose a location for a log file to be written using this file save dialog. When the Execute Command Buffer button is pressed, the script will run and the script, along with resulting data read back during the script, will be saved to the file specified. The log file is a standard text file that can be opened with any text editor, and looks much like the source script file, but with the additional information of the result of each script command executed.

The third menu item is a submenu of *Recently Opened Files*. This is simply a list of script files that have previously been opened, allowing fast access to commonly-used script files. The final menu item is *Exit*, which terminates the TLV320AIC34EVM software.

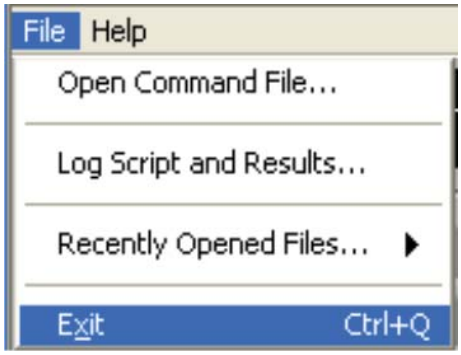


Figure 28. File Menu

Under the Help menu is an *About...* menu item which displays information about the TLV320AIC34EVM software.

The actual USB protocol used as well as instructions on writing scripts are detailed in the following subsections. While it is not necessary to understand or use either the protocol or the scripts directly, understanding them may be helpful to some users.

Appendix A EVM Connector Descriptions

This appendix contains the connection details for each of the main header connectors on the EVM.

A.1 Analog Interface Connectors

A.1.1 Block B Analog Dual Row Header Details (J13 and J14)

For maximum flexibility, the TLV320AIC34EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J13 and J14. These headers/sockets provide access to the analog input and output pins of the device. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table A-1 summarizes the analog interface pinout for the TLV320AIC34EVM..

Table A-1. Block B Analog Interface Pin Out

PIN NUMBER	SIGNAL	DESCRIPTION
J13.1	HPLCOM_B	High Power Output Driver (Left Minus or Multifunctional)
J13.2	HPLOUT_B	High Power Output Driver (Left Plus)
J13.3	HPRCOM_B	High Power Output Driver (Right Minus or Multifunctional)
J13.4	HPROUT_B	High Power Output Driver (Right Plus)
J13.5	LINE1LM_B	MIC1 or LINE1 Analog Input (Left Minus or Multifunctional)
J13.6	LINE1LP_B	MIC1 or LINE1 Analog Input (Left Plus or Multifunctional)
J13.7	LINE1RM_B	MIC1 or LINE1 Analog Input (Right Minus or Multifunctional)
J13.8	LINE1RP_B	MIC1 or LINE1 Analog Input (Right Plus or Multifunctional)
J13.9	AGND	Analog Ground
J13.10	MIC3R_B	MIC3 Input (Right or Multifunctional)
J13.11	AGND	Analog Ground
J13.12	MIC3L_B	MIC3 Input (Left or Multifunctional)
J13.13	AGND	Analog Ground
J13.14	MICBIAS_B	Microphone Bias Voltage Output
J13.15	NC	Not Connected
J13.16	MICDET_B	Microphone Detect
J13.17	AGND	Analog Ground
J13.18	NC	Not Connected
J13.19	AGND	Analog Ground
J13.20	NC	Not Connected
J14.1	LINE2RM_B	MIC2 or LINE2 Analog Input (Right Minus or Multifunctional)
J14.2	LINE2RP_B	MIC2 or LINE2 Analog Input (Right Plus or Multifunctional)
J14.3	LINE2LM_B	MIC2 or LINE2 Analog Input (Left Minus or Multifunctional)
J14.4	LINE2RP_B	MIC2 or LINE2 Analog Input (Left Plus or Multifunctional)
J14.5	MONO_LOP_B	Mono Line Output (Plus)
J14.6	MONO_LOM_B	Mono Line Output (Minus)
J14.7	LEFT_LOP_B	Left Line Output (Plus)
J14.8	LEFT_LOM_B	Left Line Output (Minus)
J14.9	AGND	Analog Ground
J14.10	RIGHT_LOP_B	Right Line Output (Plus)
J14.11	AGND	Analog Ground
J14.12	RIGHT_LOM_B	Right Line Output (Minus)
J14.13	AGND	Analog Ground
J14.14	NC	Not Connected
J14.15	NC	Not Connected
J14.16	NC	Not Connected

Table A-1. Block B Analog Interface Pin Out (continued)

PIN NUMBER	SIGNAL	DESCRIPTION
J14.17	AGND	Analog Ground
J14.18	NC	Not Connected
J14.19	AGND	Analog Ground
J14.20	NC	Not Connected

A.1.2 Block A Analog Input/Output Connectors

In addition to the analog headers, the analog inputs and outputs may also be accessed through alternate connectors, either screw terminals or audio jacks. The stereo microphone input is also tied to J6 and the stereo headphone output (the HP set of outputs) is available at J7.

Table A-2 summarizes the analog input/output connectors available for Block A.

Table A-2. Block A Analog Input/Output Connectors

DESIGNATOR	Description	PIN 1	PIN 2	PIN3
J1	2-Connector Screw Terminal Input	LINE1LP_A	LINE1LM-A	NA
J2	2-Connector Screw Terminal Input	LINE1RP_A	LINE1RM_A	NA
J3	2-Connector Screw Terminal Input	LINE2LP_A	LINE2LM_A	NA
J4	2-Connector Screw Terminal Input	LINE2RP_A	LINE2RM_A	NA
J5	3-Connector Screw Terminal Input	MIC3L_A IN LEFT	MIC3R_A IN RIGHT	AGND
J6	Audio 3.5mm Input Jack	MIC3L_A IN LEFT	MIC3R_A IN RIGHT	AGND
J7	Audio 3.5mm Output Jack	(+) HPLOUT_A	(+) HPROUT_A	AGND
J8	2-Connector Screw Terminal Output	MONO OUT_A -	MONO OUT_A +	NA
J9	2-Connector Screw Terminal Output	LEFT OUT_A-	LEFT OUT_A +	NA
J10	2-Connector Screw Terminal Output	RIGHT OUT_A -	RIGHT OUT_A +	NA
J11	3-Connector Screw Terminal Output	(+) HPLOUT_A	(-) HPLCOM_A	AGND
J12	3-Connector Screw Terminal Output	(+) HPROUT_A	(-) HPRCOM_A	AGND

A.2 Block A and Block B Digital Interface Connectors (J16 and J17)

The TLV320AIC34EVM is designed to easily interface with multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J16 and J17. These headers/sockets provide access to the digital control and serial data pins of the device. Consult Samtec at www.samtec.com or call 1-800- SAMTEC-9 for a variety of mating connector options. Table A-3 summarizes the digital interface pinout for the TLV320AIC34EVM.

Table A-3. Block A and Block B Digital Interface Pin Out

PIN NUMBER	SIGNAL	DESCRIPTION
J16.1	NC	Not Connected
J16.2	GPIO1_A	Block A General Purpose Input/Output #1
J16.3	NC	Not Connected
J16.4	DGND	Digital Ground
J16.5	NC	Not Connected
J16.6	GPIO2_A	Block A General Purpose Input/Output #2
J16.7	NC	Not Connected
J16.8	RESET INPUT	Reset signal input to AIC34EVM (/RESET_A and /RESET_B tied together)
J16.9	NC	Not Connected
J16.10	DGND	Digital Ground
J16.11	NC	Not Connected
J16.12	NC	Not Connected
J16.13	NC	Not Connected
J16.14	AIC34 $\overline{\text{RESET}}$	Reset
J16.15	NC	Not Connected
J16.16	SCL	I^2C Serial Clock
J16.17	NC	Not Connected
J16.18	DGND	Digital Ground
J16.19	NC	Not Connected
J16.20	SDA	I^2C Serial Data Input/Output
J17.1	NC	Not Connected
J17.2	NC	Not Connected
J17.3	BCLK_A	Block A Audio Serial Data Bus Bit Clock (Input/Output)
J17.4	DGND	Digital Ground
J17.5	BLK_B	Block B Audio Serial Data Bus Bit Clock (Input/Output)
J17.6	NC	Not Connected
J17.7	WCLK_A	Block A Audio Serial Data Bus Word Clock (Input/Output)
J17.8	NC	Not Connected
J17.9	WCLK_B	Block B Audio Serial Data Bus Word Clock (Input/Output)
J17.10	DGND	Digital Ground
J17.11	DIN_A	Block A Audio Serial Data Bus Data Input (Input)
J17.12	DIN_B	Block B Audio Serial Data Bus Data Input (Input)
J17.13	DOUT_A	Block A Audio Serial Data Bus Data Output (Output)
J17.14	DOUT_B	Block B Audio Serial Data Bus Data Output (Output)
J17.15	NC	Not Connected
J17.16	SCL	I^2C Serial Clock
J17.17	MCLK_A	Block A Master Clock Input
J17.18	DGND	Digital Ground
J17.19	MCLK_B	Block B Master Clock Input
J17.20	SDA	I^2C Serial Data Input/Output

Note that J17 comprises the signals needed for an I^{2}S™ serial digital audio interface; the control interface (I^{2}C™ and $\overline{\text{RESET}}$) signals are routed to J16. I^{2}C is actually routed to both connectors; however, the device is connected only to J16.

A.3 Power Supply Connector Pin Header, J15

J15 provides connection to the common power bus for the TLV320AIC34EVM. Power is supplied on the pins listed in Table A-4.

Table A-4. Power Supply Pin Out

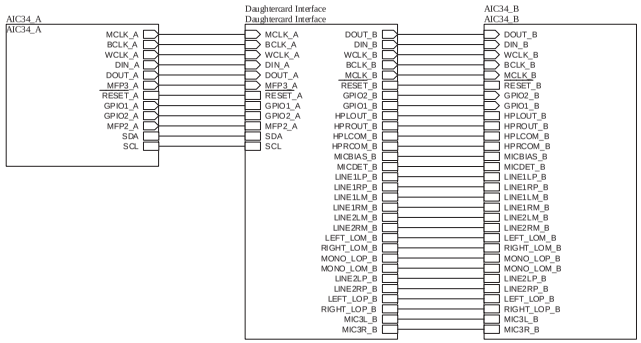
SIGNAL	PIN NUMBER		SIGNAL
NC	J15.1	J15.2	NC
+5VA	J15.3	J15.4	NC
DGND	J15.5	J15.6	AGND
DVDD (1.8V)	J15.7	J15.8	NC
IOVDD (3.3V)	J15.9	J15.10	NC

The TLV320AIC34EVM-K motherboard (the USB-MODEVM Interface board) supplies power to J15 of the TLV320AIC34EVM. Power for the motherboard is supplied either through its USB connection or via terminal blocks on that board.

Appendix B TLV320AIC34EVM Schematic

The schematic diagram for the modular TLV320AIC34EVM is provided as a reference.

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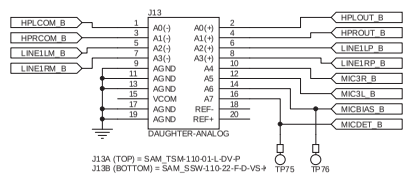
TEXAS INSTRUMENTS

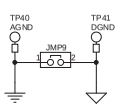
DATA ACQUISITION PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

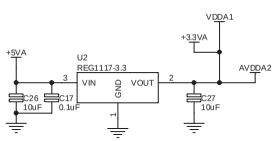
6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

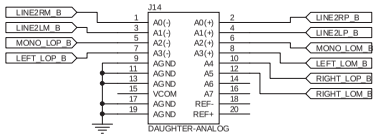
ENGINEER **FRYE D. ZERKETTS**	TITLE **untitled**		
DRAWN BY **I. C. SPOTTS**			
DOCUMENT CONTROL NO.**1234567**	SIZE **B**	DATE **dd MMM yyyy**	REV **A**
SHEET **1** OF **1**	FILE **???**		

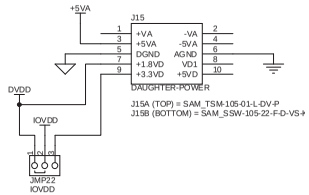
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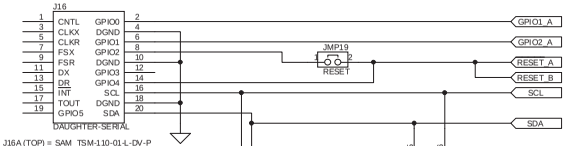


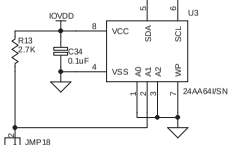


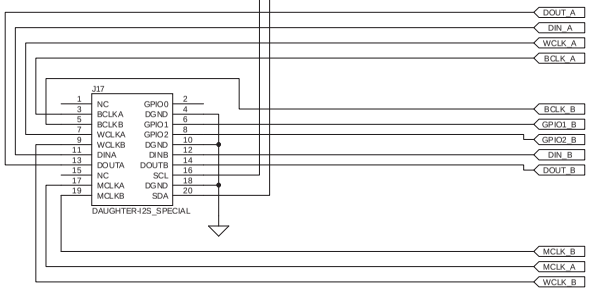










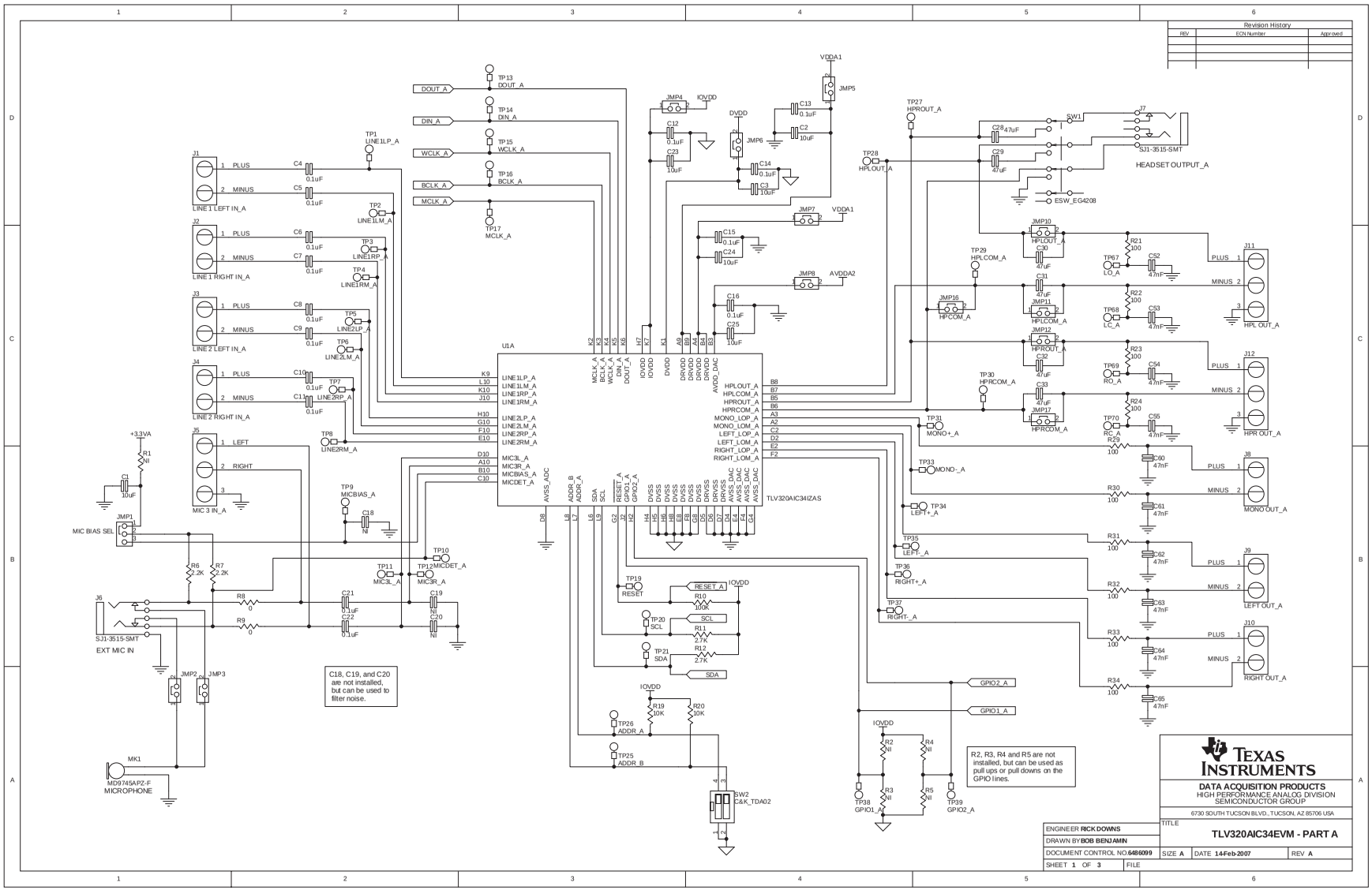


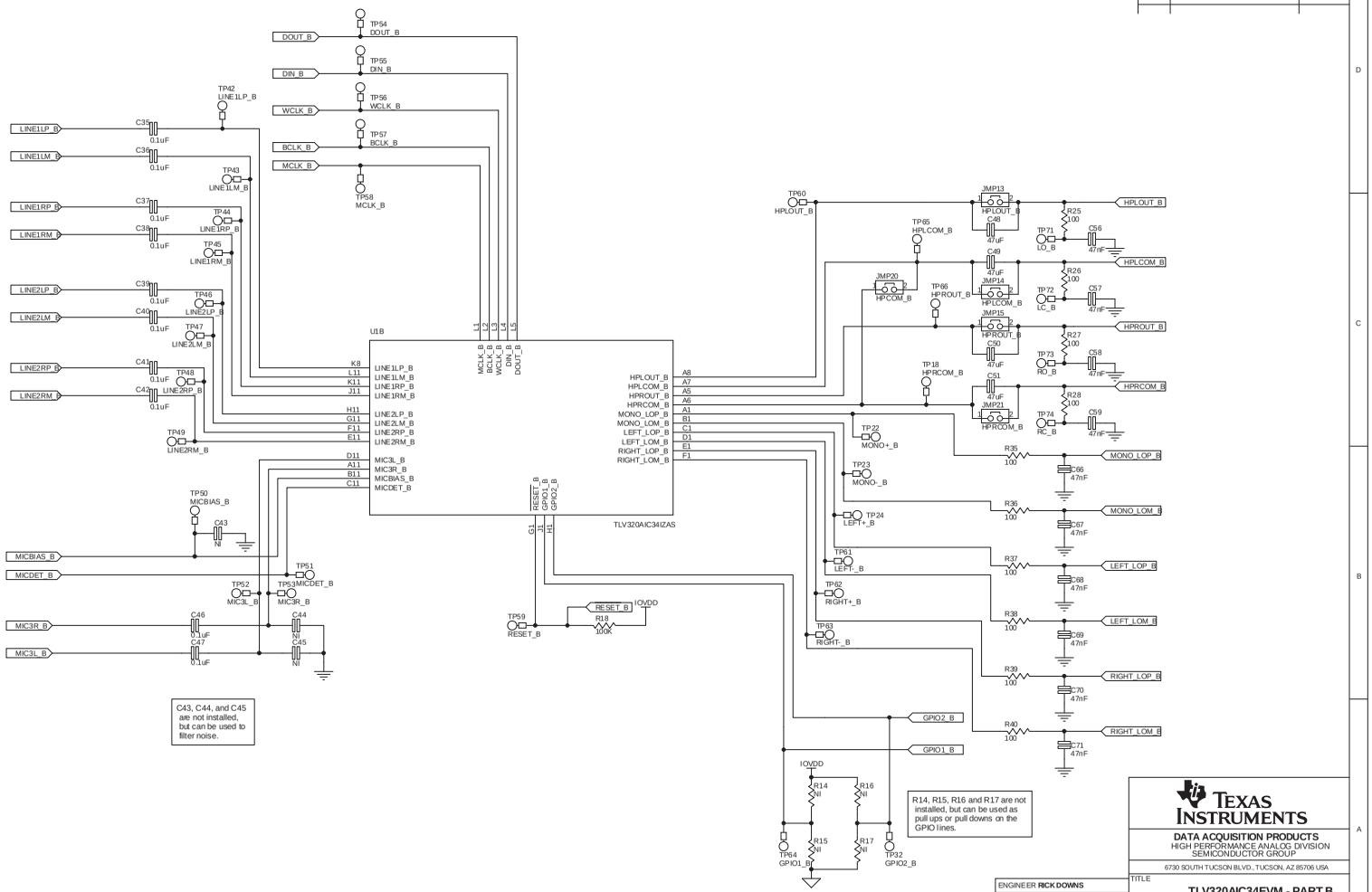
TEXAS INSTRUMENTS

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6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

ENGINEER **RICK DOWNS**	TITLE **TLV320AIC34EVM INTERFACE**		
DRAWN BY **BOB BENJAMIN**			
DOCUMENT CONTROL NO.**6486099**	SIZE **B**	DATE **14-Feb-2007**	REV **A**
SHEET **3** OF **3**	FILE		


Revision History
REV
ECN Number
Approved
DOUT_A
DIN_A
WCLK_A
BCLK_A
MCLK_A
TP13 DOUT_A
TP14 DIN_A
TP15 WCLK_A
TP16 BCLK_A
TP17 MCLK_A
TP1 LINE1LP_A
TP2 LINE1LM_A
TP3 LINE1RP_A
TP4 LINE1RM_A
TP5 LINE2LP_A
TP6 LINE2LM_A
TP7 LINE2RP_A
TP8 LINE2RM_A
J1 PLUS MINUS LINE 1 LEFT IN_A
J2 PLUS MINUS LINE 1 RIGHT IN_A
J3 PLUS MINUS LINE 2 LEFT IN_A
J4 PLUS MINUS LINE 2 RIGHT IN_A
J5 LEFT RIGHT MIC 3 IN_A
C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C11 0.1uF
+3.3VA
R1 NI
C1 10uF
JMP1 MIC BIAS SEL
TP9 MICBIAS_A
C18 NI
TP10 MICDET_A
TP11 MIC3L_A
TP12 MIC3R_A
R6 2.2K
R7 2.2K
R8 0
R9 0
J6 SJ1-3515-SMT EXT MIC IN
C21 0.1uF
C22 0.1uF
C19 NI
C20 NI
C18, C19, and C20 are not installed, but can be used to filter noise.
JMP2
JMP3
MK1 MD9745APZ-F MICROPHONE
U1A
TLV320AIC34IZAS
LINE1LP_A
LINE1LM_A
LINE1RP_A
LINE1RM_A
LINE2LP_A
LINE2LM_A
LINE2RP_A
LINE2RM_A
MIC3L_A
MIC3R_A
MICBIAS_A
MICDET_A
HPLOUT_A
HPLCOM_A
HPROUT_A
HPRCOM_A
MONO_LOP_A
MONO_LOM_A
LEFT_LOP_A
LEFT_LOM_A
RIGHT_LOP_A
RIGHT_LOM_A
MCLK_A
BCLK_A
WCLK_A
DIN_A
DOUT_A
IOVDD
DVDD
DRVDD
AVDD_DAC
AVSS_ADC
ADDR_B
ADDR_A
SDA
SCL
RESET_A
GPIO1_A
GPIO2_A
AVSS_DAC
JMP4 IOVDD
JMP5 VDDA1
JMP6 DVDD
JMP7 VDDA1
JMP8 AVDDA2
C12 0.1uF
C23 10uF
C13 0.1uF
C2 10uF
C14 0.1uF
C3 10uF
C15 0.1uF
C24 10uF
C16 0.1uF
C25 10uF
TP19 RESET
RESET_A
R10 10K
TP20 SCL
SCL
R11 2.7K
TP21 SDA
R12 2.7K
SDA
R19 10K
R20 10K
TP26 ADDR_A
TP25 ADDR_B
SW2 C&K_TDA02
TP27 HPROUT_A
TP28 HPLOUT_A
TP29 HPLCOM_A
TP30 HPRCOM_A
TP31 MONO+_A
TP33 MONO-_A
TP34 LEFT+_A
TP35 LEFT-_A
TP36 RIGHT+_A
TP37 RIGHT-_A
C28 47uF
C29 47uF
SW1
J7 SJ1-3515-SMT
HEADSET OUTPUT_A
ESW_EG4208
JMP10 HPLOUT_A
JMP16 HPCOM_A
JMP11 HPLCOM_A
JMP12 HPROUT_A
JMP17 HPRCOM_A
C30 47uF
C31 47uF
C32 47uF
C33 47uF
R21 100
R22 100
R23 100
R24 100
TP67 LO_A
TP68 LC_A
TP69 RO_A
TP70 RC_A
C52 47nF
C53 47nF
C54 47nF
C55 47nF
J11 PLUS MINUS HPL OUT_A
J12 PLUS MINUS HPR OUT_A
R29 100
R30 100
R31 100
R32 100
R33 100
R34 100
C60 47nF
C61 47nF
C62 47nF
C63 47nF
C64 47nF
C65 47nF
J8 PLUS MINUS MONO OUT_A
J9 PLUS MINUS LEFT OUT_A
J10 PLUS MINUS RIGHT OUT_A
R2 NI
R3 NI
R4 NI
R5 NI
TP38 GPIO1_A
TP39 GPIO2_A
R2, R3, R4 and R5 are not installed, but can be used as pull ups or pull downs on the GPIO lines.
TEXAS INSTRUMENTS
DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA
ENGINEER RICK DOWNS
DRAWN BY BOB BENJAMIN
DOCUMENT CONTROL NO. 6486099
SHEET 1 OF 3
TITLE
TLV320AIC34EVM - PART A
SIZE A
DATE 14-Feb-2007
REV A
FILE


Revision History
REV
ECN Number
Approved
DOUT_B
DIN_B
WCLK_B
BCLK_B
MCLK_B
TP54 DOUT_B
TP55 DIN_B
TP56 WCLK_B
TP57 BCLK_B
TP58 MCLK_B
U1B
TLV320AIC34IZAS
LINE1LP_B
LINE1LM_B
LINE1RP_B
LINE1RM_B
LINE2LP_B
LINE2LM_B
LINE2RP_B
LINE2RM_B
MIC3L_B
MIC3R_B
MICBIAS_B
MICDET_B
RESET_B
GPIO1_B
GPIO2_B
HPLOUT_B
HPLCOM_B
HPROUT_B
HPRCOM_B
MONO_LOP_B
MONO_LOM_B
LEFT_LOP_B
LEFT_LOM_B
RIGHT_LOP_B
RIGHT_LOM_B
IOVDD
C43, C44, and C45 are not installed, but can be used to filter noise.
R14, R15, R16 and R17 are not installed, but can be used as pull ups or pull downs on the GPIO lines.
TEXAS INSTRUMENTS
DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA
TITLE
TLV320AIC34EVM - PART B
ENGINEER RICK DOWNS
DRAWN BY BOB BENJAMIN
DOCUMENT CONTROL NO. 6486099
SIZE A
DATE 14-Feb-2007
REV A
SHEET 2 OF 3
FILE

Appendix C TLV320AIC34EVM Layout Views

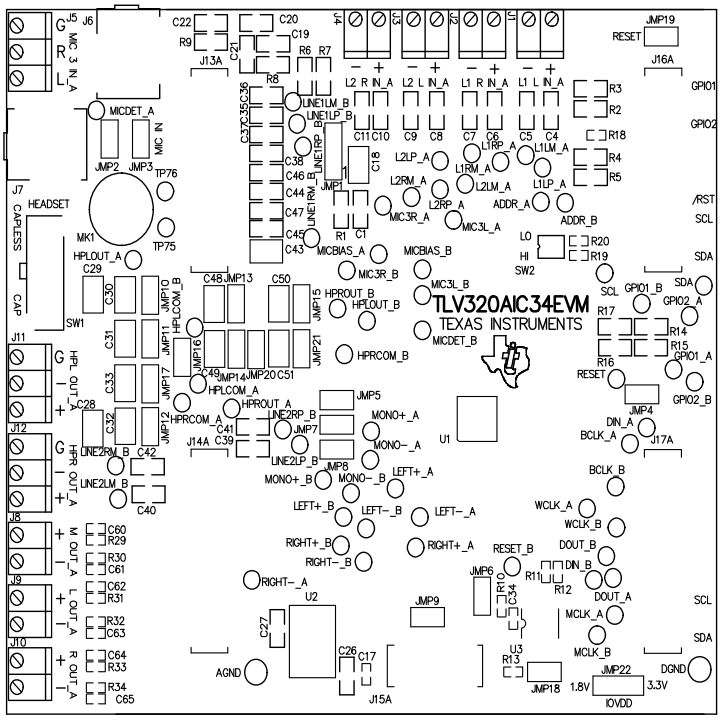


Figure C-1. Assembly layer

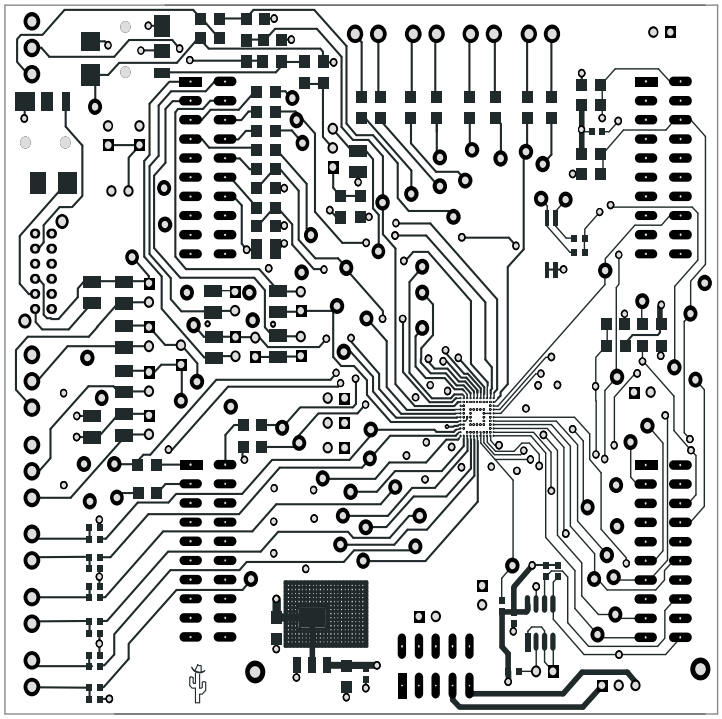


Figure C-2. Top Layer

